CURRENT-MODE ANALOG CMOS RATIONAL-POWERED FUNCTION GENERATOR

BY

ADI KURNIAWAN

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This thesis, written by **ADI KURNIAWAN** under the direction of his thesis adviser and approved by his thesis committee, has been presented to and accepted by the Dean of Graduate Studies, in partial fulfillment of the requirements for the degree of **MASTER OF SCIENCE IN ELECTRICAL ENGINEERING**.

Thesis Committee

Dr. Muhammad Taher Abuelma'atti (Adviser)

Dr. Munir A. Kulaib Al-Absi (Member)

Dr. Alaa El-Din Hussein (Member)

Dr. Ali Ahmad Al-Shaikhi
Department Chairman

Dr. Salam A. Zummo
Dean of Graduate Studies

10/5/13
Date

Dedication

I would like to dedicate my thesis to my beloved parent.
May Allah forgive my sins and the sins of them, have mercy on them as they loved me when I was a kid.

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Alhamdulillah. All the praises and thanks be to Allah that has given me the opportunity and capability to finish my study at King Fahd University of Petroleum & Minerals (KFUPM).

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LIST OF ABBREVIATIONS

BSIM:	Berkeley Short-channel IGFET Model for MOS Transistors
BJT:	Bipolar Junction Transistor
CMOS:	Complementary Metal Oxide Semiconductor
IC:	Integrated Circuit
MOS:	Metal Oxide Semiconductor
MOSFET:	The Metal Oxide Semiconductor Field-Effect Transistor
MTL:	MOS Translinear
RMSE:	Root Mean Square Error
TLP:	Translinear Principle (for BJT)
TSMC:	Taiwan Semiconductor Manufacturing Company, Limited

THESIS ABSTRACT

NAME: Adi Kurniawan

TITLE OF STUDY: Current-Mode Analog CMOS Rational-Powered Function Generator

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Analog techniques are preferably used in the computational circuits as they operate at low power, and they are relatively fast. This thesis proposes a new simpler approximation of the programmable rational powered function $y = x^a$ *using current-mode analog CMOS working in the saturation region. The proposed circuits utilize less number of components; a squaring circuit and two 8-bits programmable current mirrors with current flow direction controller. It demands less area on the chip and consumes less power compared to the previously published circuits. It uses dual voltage sources* $\pm 1.25V$ *offering compatibility to integrate with another Integrated Circuit. The proposed circuits were successfully simulated in T-Spice using 0.18* μm *CMOS technology. The performance of the circuits was confirmed by varying the temperature from* $-25\,^{\circ}\mathrm{C}$ *to* $75\,^{\circ}\mathrm{C}$ *and Monte Carlo analysis. The Layout design of the circuits was carried out to check the feasibility of the circuit in fabrication.*

ملخص الرسالة

الاسم الكامل: أَدِي كُورْنِيَاوَان ويرمان

عنوان الرسالة: مُولّد الدوال نسبيّ القدرة باستخدام CMOS ذي الوضع التياريّ

التخصص: الهندسة الكهربائية

تاريخ الدرجة العلمية: أبريل ٢٠١٨

يُفضل استخدام التقنيات التناظرية في الدارات الحسابية؛ حيث أنها تعمل على طاقةٍ منخفضةٍ، وهي سريعةٌ نسبياً. تقترح هذه الرسالة تقريباً جديداً أبسط للدالة: $y = x^a$ نسبية القدرة والقابلة للبرمجة، باستخدام شبه موصلٍ معدنيٍّ متكاملٍ مغطى بالأكسيد CMOS تناظريّ ذي الوضع التياريّ يعمل في منطقة التشبع. تستخدم الدارات المقترحة عدداً أقل من المكونات؛ دائرة تربيعٍ و مرآتي تيّارٍ ذواتيْ ٨-بتّات قابلتين للبرمجة مع جهاز تحكمٍ لاتجاه تدفق التيّار. ولديك فهي تتطلب مساحةً أقل على الشريحة و تستهلك طاقةً أقل مقارنةً بالدارات المنشورة سابقاً. وتستخدم مصادر جهدٍ مزدوجٍ ($\pm$ 1.25 فولت) مما يوفّر التوافق للاندماج مع الدوائرِ متكاملةٍ أخرى. تم التحقق من أداء التطبيق المقترح من خلال تغيير درجة الحرارة من 25°C- إلى 75°C+ وتحليل مونتي كارلو Monte Carlo في برنامج T-Spice باستخدام تقنية 0.18 µm CMOS. تم تنفيذ تصميم تخطيط الدائرة للتأكد من جدوى الدارة عند التصنيع.

CHAPTER 1

INTRODUCTION

1.1 Background

Analog implementation of signal processing circuits provides higher speed operation, lower power consumption, and smaller size on the chip compared to digital implementation. But analog non-linear signal processing suffers from its limited accuracy. However, analog non-linear signal processing is still used for applications where speed rather than accuracy is the most important issue, the examples include medical equipment and telecommunications [1, 2].

One of the essential computational circuits in analog signal processing is the rational powered or fractional powered functions (x^a). There are several applications that benefit from this block like in electronics communication as Root Mean Square (RMS) indicator [3], modeling telecommunication [4, 5], fuzzy logic controller [6–10], and wireless image sensor networks [11, 12].

On the other hand, there are many approaches to design analog computational circuits. The translinear principle is one of the famous methods for realizing it. This principle has caught many interests as it is not only applicable to Bipolar Junction Transistor (BJT) but also to Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET).

1.1.1 BJT Translinear Principle

The translinear principle (TLP) was first introduced by Gilbert in 1975 [13]. It offers a simple method of realizing complex mathematical functions with a few number of transistors. Gilbert basically proposes The Translinear Principle for BJT transistor. Figure 1.1 shows the basic BJT translinear loop circuit.

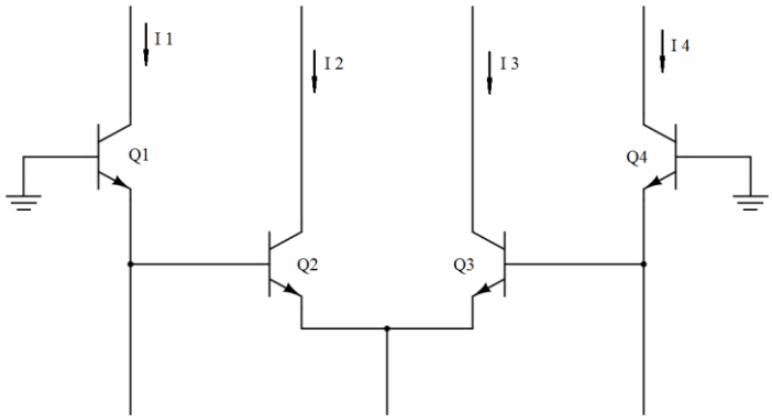


Figure 1.1: Translinear loop of BJT.

The translinear principle states that if a circuit has an even number PN junctions with equal number of clockwise and counterclockwise oriented, the product of the currents in one half is equal to the products of the currents in the other half. This can be shown as follows.

In a closed loop,

$$\sum clockwise V_{BE} = \sum counterclockwise V_{BE} \tag{1.1}$$

But it is known that for a bipolar transistor [14],

$$I_C = I_S \exp\left(V_{BE}/V_T\right) \tag{1.2}$$

Thus,

$$V_{BE} = V_T.ln\frac{I_C}{I_S} \tag{1.3}$$

where I_S is the reverse bias saturation current, I_C is the collector current, V_{BE} is the voltage between the base and emitter, and V_T is the thermal voltage.

By combining equation (1.1) and (1.3),

$$\sum clockwise V_T.ln\frac{I_C}{I_S} = \sum counterclockwise V_T.ln\frac{I_C}{I_S} \tag{1.4}$$

By assuming all transistor are identical, then equation (1.4) reduces to,

$$\prod clockwise I_C = \prod counterclockwise I_C \tag{1.5}$$

1.1.2 MOSFET Translinear Principle

MOSFET is far away more popular than BJT. The main reason is that the fabrication cost for MOSFET is cheaper than BJT. In addition, MOSFET is much smaller in terms of size than BJT. The translinear principle also can be applied in a similar way to MOSFET operated in the subthreshold region (weak inversion) [15–17]. In this region, the drain current I_D has an exponential relation with V_{GS}. The MOSFET drain current in subthreshold region is defined as follows,

$$I_D = \frac{W}{L} I_O \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) \tag{1.6}$$

where W is the channel width and L is the channel length, V_{TH} is threshold voltage, V_T is thermal voltage, the pre-factor I_O is the subthreshold saturation current which dependent on process parameters and the bulk-source voltage, $I_O\frac{W}{L}$ is the current that flows when $V_{GS} = V_{TH}$, and n is the subthreshold exponential slope factor.

When drain to source voltage V_{DS} is large enough compare to thermal voltage V_T, equation (1.6) can be simplified as follows,

$$I_D = \frac{W}{L} I_O \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right) \tag{1.7}$$

Then, V_{GS} can be written as follows,

$$V_{GS} = V_{TH} + nV_T \ln\left(\frac{I_D}{I_O}\frac{L}{W}\right) \tag{1.8}$$

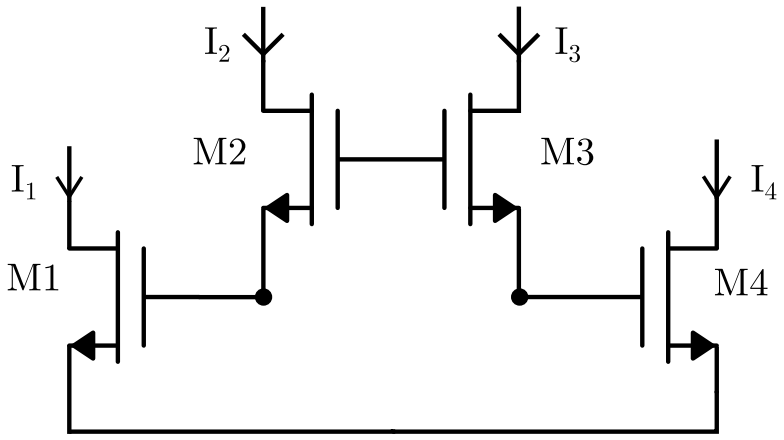


Figure 1.2: Translinear loop of MOSFET.

Applying KVL in the translinear loop, where half of the MOSFETs are clockwise oriented and the other half are counterclockwise oriented, then

$$\sum clockwise V_{GS} = \sum counterclockwise V_{GS} \tag{1.9}$$

By substituting the value of V_{GS} from equation (1.8) to equation (1.9) yields,

$$\sum clockwise\left(V_{TH}+nV_T\ln\left(\frac{I_D}{I_O}\frac{L}{W}\right)\right)=\sum counterclockwise\left(V_{TH}+nV_T\ln\left(\frac{I_D}{I_O}\frac{L}{W}\right)\right) \tag{1.10}$$

By assuming that all the transistors are identical, equation (1.10) can be reduced to:

$$\prod clockwise I_D=\prod counterclockwise I_D \tag{1.11}$$

In reference of Figure 1.2, equation (1.11) can be written as follows,

$$I_{D1}I_{D2}=I_{D3}I_{D4} \tag{1.12}$$

MOSFET circuits work in subthreshold region promises ultra low-power consumption analog circuits suitable for the battery-powered applications. There are several analog computational circuits exploiting the advantage of translinear principle in weak inversion [5, 18–20]. However, the speed and dynamic range of circuits working in the subthreshold region would be a limitation for a general application of such circuits.

The translinear principle for MOSFET can be naturally extended for circuits working in the strong inversion region. This generalization of MOSFET translinear principle was derived by Seevinck [21]. Gilbert introduced new term voltage-translinear (VTL) to distinguish with classical term MOS-translinear (MTL) which might refer to either translinear principle using transistor working in the strong inversion or classical subthreshold region [22, 23]. In strong inversion, the circuit will work based on the square-law characteristics rather than exponential characteristics relation like in BJT and MOSFET in subthreshold region. The drain current function I_D of MOSFET

working in the saturation region can be expressed as follows,

$$I_D = \frac{K}{2}(V_{GS} - V_{TH})^2(1 + \lambda(V_{DS})) \tag{1.13}$$

where $K = \mu C_{ox}(W/L)$ is transconductance parameter of the transistor.

By selecting long channel transistor, the channel length modulation effect can be minimized. Hence, equation (1.13) can be simplified as follows,

$$I_D = \frac{K}{2}(V_{GS} - V_{TH})^2 \tag{1.14}$$

Equation (1.14) can be rearranged to get the relation of V_{GS} as follows,

$$V_{GS} = V_{TH} + \sqrt{\frac{I_D}{K}} \tag{1.15}$$

Applying KVL in the transistor loop where half of the MOSFETs are clockwise oriented and the other half are counterclockwise oriented then, by substituting the value of V_{GS} from equation (1.15) to (1.9), yields:

$$\sum V_{TH} + \sqrt{\frac{I_D}{K}} = \sum V_{TH} + \sqrt{\frac{I_D}{K}} \tag{1.16}$$

By assuming the MOSFET transistors are identical then threshold voltage, V_{TH} will be equal. Equation (1.16) could be simplified to be,

$$\sum \sqrt{I_D} = \sum \sqrt{I_D} \tag{1.17}$$

In reference of Figure 1.2, equation (1.17) can be written as follows,

$$\sqrt{I_{D1}} + \sqrt{I_{D2}} = \sqrt{I_{D3}} + \sqrt{I_{D4}} \tag{1.18}$$

The Translinear Principle of BJT and MOSFET working in the subthreshold region is a product relation which can naturally develop the functions involving multiplication and division. Meanwhile, The Translinear Principle of MOSFET in the saturation region is a sum of-roots relation which provide a challenge to implement the circuit.

1.1.3 MOSFET Current-Mode Circuit

In current-mode circuit, input and output variables are currents. Circuit information is denoted by the branch currents of the circuits rather than the nodal voltages as in voltage-mode operation. Designing MOSFET current-mode circuit rapidly attract particular interest in many applications, such as in telecommunication systems, instrumentation, multiprocessors, high-speed computer interfaces and analog signal processing. The substantial reduction in the voltage supply and device threshold voltage of MOSFET have greatly affected the performance of MOSFET by reduction the dynamic range, increasing propagation delay, and reducing low noise margins. The current-mode circuits less severe affected compare to voltage-mode circuits [24]. The current mode circuit offers larger dynamic range, larger bandwidth, and lower power dissipation [4, 12, 25]. Using current-mode circuits, many functions can be designed with less number of components compared to its voltage-mode counterpart. For example, the implementation of add and subtract operation in current-mode can be easily by connecting the low impedance wire.

1.2 Motivation

Rational-powered function is one of the important computational building blocks in signal processing. Squaring and square rooting circuits are easy to implement and they are widely available in the open literature. However, for other functions; such as the power-law function, the realization may be very complex. In this thesis, a new approach for realizing a rational-powered function is investigated. The new approach uses less number of basic building blocks. Thus, requires less area on the chip and consumes less power. The new approach is expected to be easily implemented using modern MOSFET technologies.

1.3 Problem Definition

Analog computational circuits are important blocks in signal processing. It is desirable to obtain less complex circuit that can perform complicated functions with an acceptable error. The goal of this thesis to design and simulate simple analog computational circuits to perform the rational-powered functions by utilizing current-mode MOSFET working in saturation region.

1.4 Thesis Outline

The thesis is divided into five main chapters. Firstly, as an introduction, it will discuss the background, motivation, problem definition and an outline of the thesis. The second chapter discusses the previous works in the literature. Proposed circuits are introduced in the third chapter whereas the fourth chapter, will show and discuss the simulation results. Conclusion and recommendation are presented in the fifth chapter.

CHAPTER 2

LITERATURE REVIEW

There are many approaches to design the rational powered function generator [3,4,6–10, 12]. The authors in [3,4] use breadboarded IC to implement true-powered functions. The authors in [3] used a voltage-mode OTA-based circuit to design few powered functions such as squaring circuit, cube-law circuit, and square rooting circuit. The authors in [4] used BJT transistors to realize power-law function as shown in Figure 2.1. Applying the translinear principle to transistor Q5 to Q8 of figure 2.1a yields

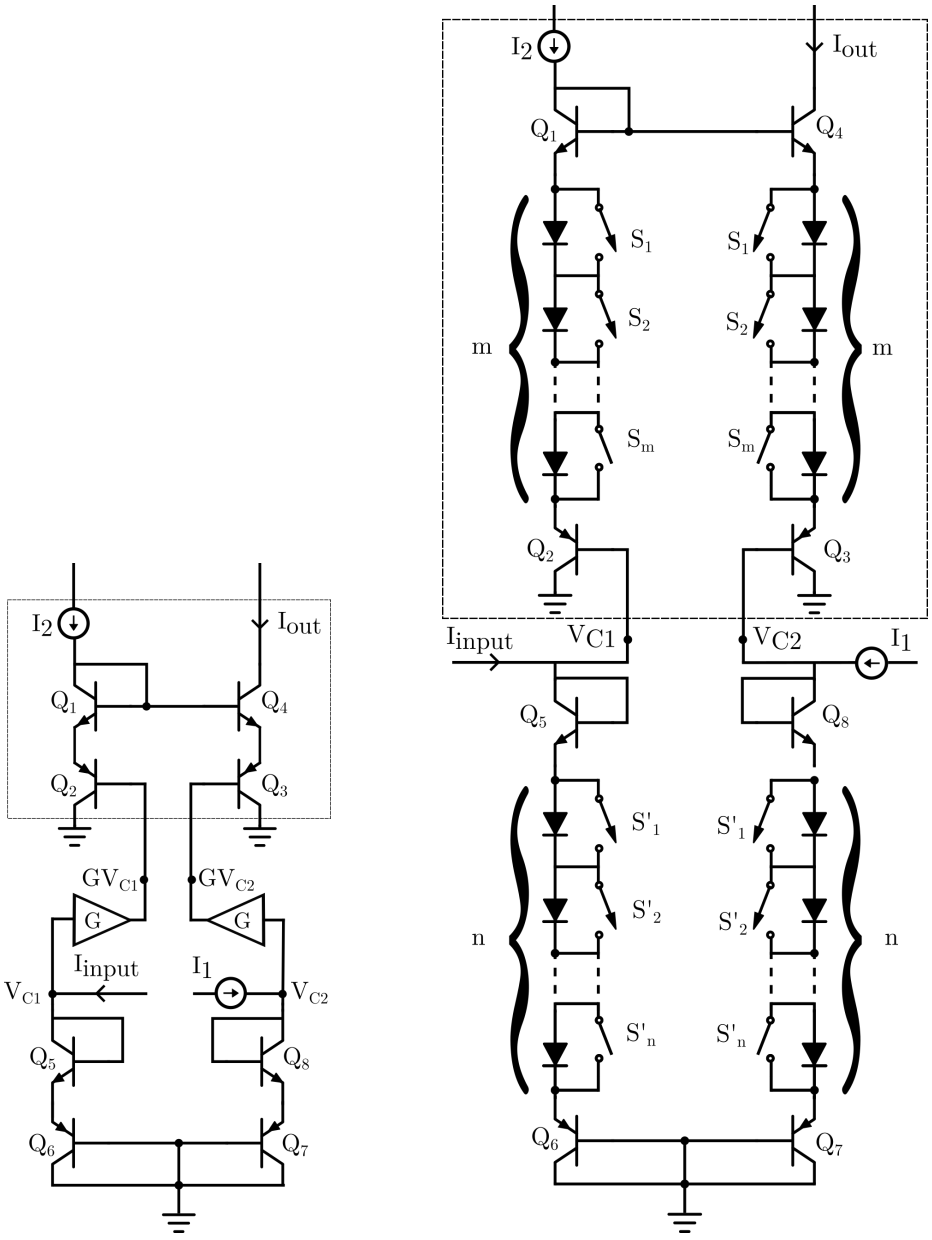
$$V_{C1} - V_{C2} = V_T \ln \left(\frac{I_{input}}{I_1} \right)^2 \tag{2.1}$$

where V_T is the termal volage. The same principle can be applied to the translinear loop of transistor Q1 to Q4, yields:

$$G(V_{C1} - V_{C2}) = V_T \ln \left(\frac{I_{out}}{I_2} \right)^2 \tag{2.2}$$

Hence, combining Equation (2.1) amd (2.2), yields

$$I_{out} = I_2 \left(\frac{I_{out}}{I_1} \right)^G \tag{2.3}$$



(a) General power-law function circuit (b) Programmable power-law circuit

Figure 2.1: Powered function generator proposed by [4].

If G can be modified as the form of the ratio of two integers, the circuit can realize a wide-range of power-law function. One way to implement this method is shown in Figure 2.1. The proposed circuit can implement a digitally-programmable current-mode power-law function generator as a form of integer powers and ratio of two integers (equation (2.4)). The power can be adjusted by controlling the switches.

$$I_{OUT} = \left(\frac{I_{IN}}{I_1}\right)^{\frac{n+2}{m+2}} I_2 \tag{2.4}$$

The recent approach is to use MOSFET to implement rational powered functions. It compromises simplicity and possibility to fabricate. The authors of [5] propose fractional functions generator using floating gate CMOS in the subthreshold region. They use programmable capacitance matrix with switches to control the power. Working in subthreshold region offers an ultra low-power and low-voltage circuit. However, as mentioned earlier, it has the limitation in speed which may not be suitable for the general applications.

Several methods to map specific function x to x^a using CMOS in saturation region were reported in the literature. Chen et.al. [6] realized some limited power of: 0.25, 0.5, 0.75, 1.25, 1.5, 2, and 4 by using only G-mean and squarer-divider (sq/d) circuit. Combining these core blocks can generate variations of power. Cascading two G-mean blocks will produce a power of 0.25. Furthermore, cascading two sq/d blocks will produce a power of 4. Mottaghi et al. [7] try to improve the structure proposed by Chen et.al. [6], hence it can provide more powers. They proposed rational power function from 0.125 to 4 with a resolution of 0.125. However, this work has complex structure by cascading couple of square rooting circuits which will dissipate huge power. The authors in [8, 12] use the properties of logarithm technique to implement rational power function. They

use block function of power Napier's constant e^x and natural logarithmic $ln(x)$ then cascade them together using standard CMOS technology as shown in equation (2.5),

$$x^a = \exp\left(a.\ln(x)\right) \tag{2.5}$$

Nevertheless, in the saturation region, a logarithmic function cannot be naturally derived from the basic relationship I-V such as BJT or CMOS in subthreshold region [5]. Hence, they need to use an approximation of logarithmic and exponential functions.

Naderi et al. [8] approximate logarithmic and exponential function by using only square rooting and squaring terms as shown in equations (2.6) and (2.7) which is simple and easy to implement.

$$|\ln(x)| = -0.84x^2 + 4.8x - 8.4\sqrt{x} + 4.5 \tag{2.6}$$

$$e^{-x} = 0.19x^2 - 0.82x + 1 = (0.43x)^2 - 0.82x + 1 \tag{2.7}$$

To realize different power functions, they control it by multiplying the output current of $\ln(x)$ by using current mirror with selectable gain as seen in Figure 2.2.

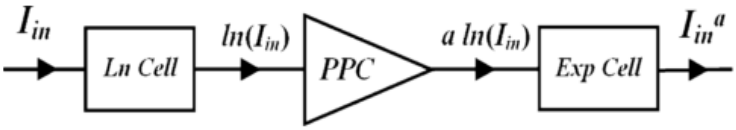


Figure 2.2: Rational powered function reported in [8].

The resolution of power is determined by Power Programming Circuit (PPC) block. They attained it by using 7 bits programming code with the resolution of 0.03125.

Lin et al. [12] use the same basic approach of equation (2.5) but they prefer to define

the power as fraction number n/m as in equation (2.8). They propose a compact circuit to approximate the rational powered function using less transistors.

$$x^{m/n} = \exp\left(\ln(x^{n/m})\right) \tag{2.8}$$

The logarithmic and exponential functions are approximated with the following equations based on second-order Taylor expansion at $x = a_0$ and $x = b_0$ respectively for $\ln(x)$, and e^x,

$$\ln(x) \cong -2\left(1 - \frac{2}{a_0}\right)^2 + \ln a_0 + 0.5 \tag{2.9}$$

$$e^y \cong \frac{\exp(b_0)}{2}(1 - b_0)^2\left(1 + \frac{y}{1 - b_0}\right)^2 + \frac{\exp(b_0)}{2} \tag{2.10}$$

The authors of [12] proposed circuits in Figure 2.3 to realize the equation (2.9) and (2.10).

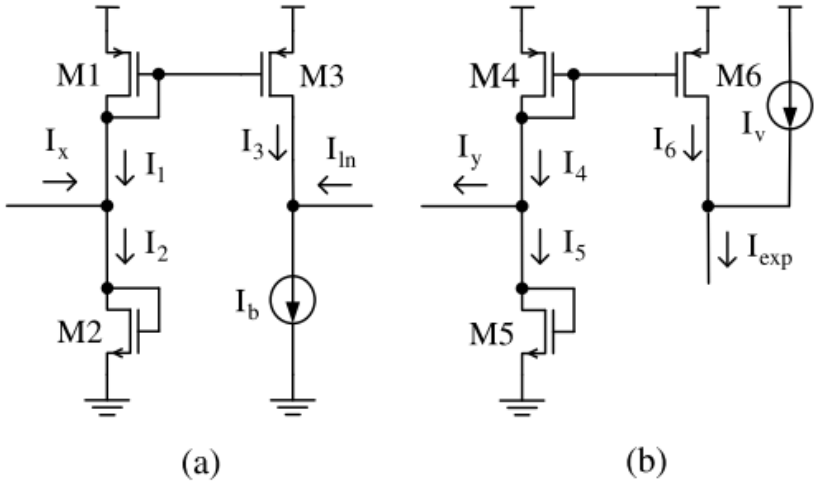


Figure 2.3: Second-order Taylor expansion circuit for natural logarithm (a) and exponential circuit (b) reported in [12].

They use back-to-back connection proposed in [26] to achieve quadratic function as

a core circuit as shown in Figure 2.4.

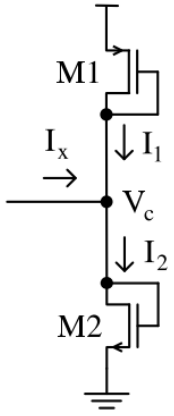


Figure 2.4: Basic square circuit from [26].

From Figure 2.4, the relation of the drain currents of M1 and M2 in the saturation region can be expressed as:

$$I_1 = K_p(V_{gs} - |V_{tp}|)^2 = K_p(V_{DD} - V_c - |V_{tp}|)^2 \tag{2.11}$$

$$I_2 = K_n(V_{gs} - V_{tn})^2 = K_n(V_c - V_{tn})^2 \tag{2.12}$$

Assuming transconductance parameter for M1 and M2 are equal, $K_p = K_n = K$, then V_c can be expressed as:

$$V_c = \frac{(V_{DD} - V_c + |V_{tp}|)}{2} + \frac{I_x}{2K(V_{DD} - |V_{tp}| - V_{tn}}) \tag{2.13}$$

By substituting the value of V_c in equation (2.13) to equation (2.11) and (2.12), then I_1 and I_2 to I_x as square-law function can be expressed as follows:

$$I_1 = K\left(\frac{(V_{DD} - |V_{tp}| - V_{tn})}{2} - \frac{I_x}{2K(V_{DD} - |V_{tp}| - V_{tn})}\right) \tag{2.14}$$

$$I_2 = K\left(\frac{(V_{DD} - |V_{tp}| - V_{tn})}{2} + \frac{I_x}{2K(V_{DD} - |V_{tp}| - V_{tn})}\right) \tag{2.15}$$

Equation (2.13), (2.14), and (2.15) can be written as follows,

$$I_1 = K{V_0}^2\left(1 - \frac{I_x}{4K{V_0}^2}\right) \tag{2.16}$$

$$I_2 = K{V_0}^2\left(1 + \frac{I_x}{4K{V_0}^2}\right) \tag{2.17}$$

$$V_c = V_0 + V_{tn} + \frac{I_x}{4K{V_0}^2} \tag{2.18}$$

where $V_0 = \frac{(V_{DD} - |V_{tp}| - V_{tn})}{2}$.

In reference of Figure 2.3a, if I_3 is mirrored from I_1 with scale factor 2, I_{ln} will be $-2I_1 + I_b$. Then, from equation (2.16):

$$I_{ln} = -2KV_0^2\left(1 - \frac{I_x}{4K{V_0}^2}\right)^2 + I_b \tag{2.19}$$

Equation (2.19) can be compared to Taylor approximation of natural logarithm in equation (2.9), by assuming $I_{ln} = I_0 \ln x$, as follows:

$$-2KV_0^2\left(1 - \frac{I_x}{4K{V_0}^2}\right)^2 + I_b = -2I_0\left(1 - \frac{x}{2{a_0}^2}\right)^2 + I_0(\ln a_0 + 0.5) \tag{2.20}$$

From equation (2.20), it is obvious that: $I_0 = KV_0^2, I_b = I_0(\ln a_0 + 0.5)$, and

$$x = \frac{a_0 I_x}{2I_0} \tag{2.21}$$

By using the same principle, in Figure 2.3b, suppose that I_{exp} has the characteristic of $\exp y$, that is $I_{exp} = I_u \exp(y)$ where I_u is a constant current. If I_6 is mirrored from

I_4 with same scale, then I_{exp} will be $I_4 + I_v$, thus

$$I_{exp} = I_u e^y = K'V_0^2 \left(1 + \frac{I_y}{4K'{V_0}^2}\right)^2 + I_v \tag{2.22}$$

where the transconductance parameters of M4 and M5 are assumed to be equal as K'. Comparing equation (2.22) to Taylor approximation of exponential in equation (2.10), then

$$K'V_0^2 \left(1 + \frac{I_y}{4K'{V_0}^2}\right)^2 + I_v = I_u \frac{\exp(b_0)}{2}(1 - b_0)^2 \left(1 + \frac{y}{1 - b_0}\right)^2 + I_u \frac{\exp(b_0)}{2} \tag{2.23}$$

From equation (2.23), it is obvious that $I_u = \frac{2K'V_0^2}{((1-b_0)\exp(b_0)}$, $I_v = I_u \frac{\exp(b_0)}{2}$, and

$$y = \frac{I_y}{I_u|1 - b_0|\exp(b_0)} = \frac{|1 - b_0|I_y}{4K'{V_0}^2} \tag{2.24}$$

By combining circuit in Figure 2.3b and 2.3b by connecting node I_{ln} and I_y, the fraction-power circuit can be derived. As the transistor M1 and M2 current-mirror ratios are $2n/m$ and current I_b becomes $I_g = (n/m)I_b$, the relation of $I_3 = (2n/m)I_1$. Since $I_y = -I_3 + I_g$, I_y will be $n/m\,(-2I_1 + Ib)$. Then, the equation (2.19) can be be written as follows,

$$I_y = \frac{n}{m} I_0 \ln(x) \tag{2.25}$$

Substituting equation (2.25) to (2.24) and selecting $|1 - b_0| = 4K'{V_0}^2$ yields,

$$y = (n/m)I_0 \ln(x) \tag{2.26}$$

Substituting the value of y from equation (2.26) to (2.22) and by knowing equation

(2.8), yields,

$$I_{out} = I_u \exp(y) = I_u x^{n/m} \tag{2.27}$$

Figure 2.5 shows the proposed programmable rational function generator reported in [12]. The n/m circuit is a selectable-gamma block by connecting node A, B, and C to either V_{DD} and GND to control the power as $\frac{1}{\gamma}$. When the node is switched to V_{DD}, it will be denoted as 1, and when the node is switched to GND, it will be denoted as 0. If the scale of current mirrors M4 to M8, M4 to M9, and M4 to M10 are a, b, and c, respectively, then $I_{nm} = (A.a + B.b + C.c)\, I_0 \ln(x)$. Since $x = \frac{a_0 I_x}{2I_0}$, if $a_0 = 2$ the relation of output current, I_{out} will be as follows,

$$I_{out} = I_u \left(\frac{I_x}{I_0}\right)^{1/\gamma} \tag{2.28}$$

where $1/\gamma = (A.a + B.b + C.c)$.

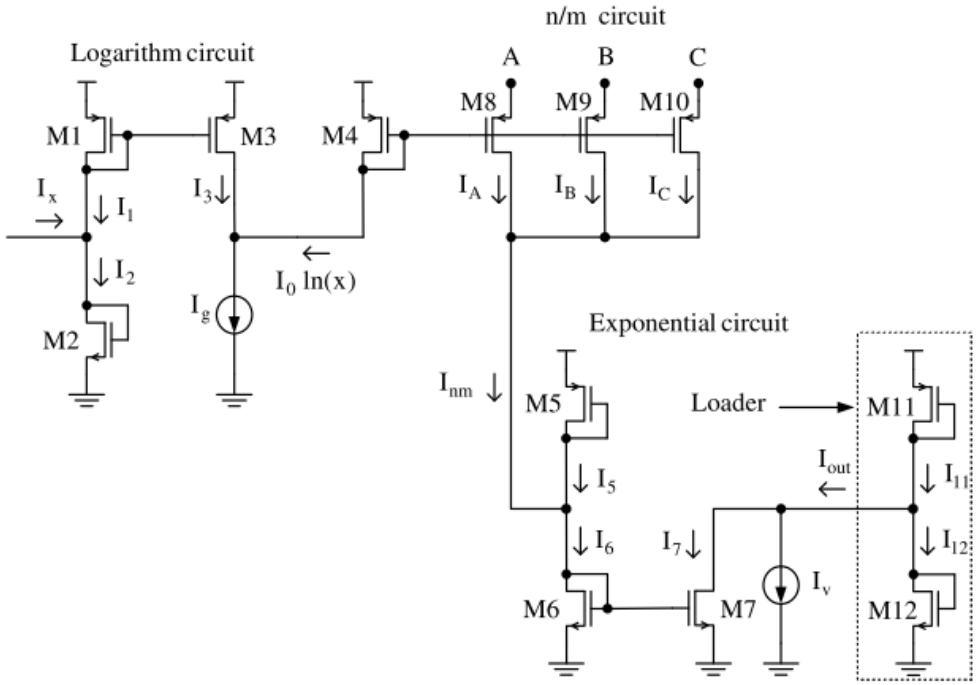


Figure 2.5: Fraction power circuit proposed in [12].

Moshfe et al. [9,10] use direct approximation by using a squarer circuit and a square rooting circuit to implement equation (2.29). They use the same approach of [8] when implementing the approximation of the natural logarithmic and the exponential function.

$$x^a \cong P_1 x^2 + P_2 x + P_3 \sqrt{x} + P_4 \tag{2.29}$$

By using a direct approximation to x^a, the error could be decreased and the resolution of power would be increased. This work is appreciable. However, the implementation of programming current mirror to implement P_1, P_2, and P_3 needs huge resources.

A comparison between some previous works of rational function generator is shown in Table 2.1.

Table 2.1: The compilation of simulation result of some proposed rational powered function generator.

Comparison Factors	[4]	[6]	[7]	[8]	[9,10]	[12]	[5]
Year	1998	2002	2007	2010	2011	2012	2017
Technology (um)	n/a	0.35	0.35	0.35	0.35	0.35	0.18
Power Supply (V)	+-5	3.3	3.3	3.3	3.3	2.5	0.5
Maximum Power consumption (uW)	n/a	n/a	5000	1050	800	970	0.48
Programming Codes (bits)	n/a	8	15	7	8	3	n/a
Power Resolution	n/m	Some limited power	0.125	0.03125	Continuous (0-2)	n/m	$\pm n/m$
RMS Error (%)	< 3	n/a	1.32	1.45	1.25	3	1.05
Size Layout (mm^2)	n/a	Core:1.55 Total:6.81	n/a	n/a	0.045	n/a	n/a
Approximation	No	No	No	Yes	Yes	Yes	No
Research Type	Simulation	Fabrication	Simulation	Simulation	Simulation	Fabrication	Simulation
Method	BJT, OpAmp, TLP	Cascade G-mean and Sq/d	Improved Cascade	MTL	MTL	MTL	FGMOS, Subthreshold

From Table 2.1, it appears that there is a room for improvement in designing rational powered function generator. This thesis is an attempt to simplify the approach of approximation of the rational power function x^a by second order polynomial, using only the squaring circuit and avoiding the square rooting circuit. The trade-off of this approach will be to allow a slight increase in the error but reduce the resources. The proposed circuit will be simulated in CMOS 0.18 μm technology. The possibility of reducing the error will be investigated.

CHAPTER 3

CIRCUIT DESIGN OF THE PROPOSED APPROXIMATION

In this thesis, a current-mode rational powered function generator will be designed. The circuit is able to map the input to the output by the function:

$$y = x^a \tag{3.1}$$

where x is the normalized input current and y is the normalized output current and a is the rational power. Second order polynomial is used to approximate the rational powered function. Hence, the proposed approximation can be expressed as follows,

$$x^a \cong \alpha x^2 + \beta x + \gamma \tag{3.2}$$

Equation (3.2) promises simpler method to implement the approximation. It shows that a squaring circuit which is the simplest component in the analog computational module and a current mirror with controllable gain is enough to realize the rational power function generator. Figure 3.1 shows the general structure of the proposed approximation of rational power function generator using second order polynomial. The

input current will be mirrored to two sides. The first one will be squared by a squaring circuit then multiplied by a gain of α. Another input current will be multiplied by a gain of β. The result will be combined with some constant current γ. The coefficient α, β and γ can be varied depending on the rational power a. Obviously, using a simpler method to approximate a function leads to an increase in the error. The performance of this approximation will be investigated for a between 0 to 4.

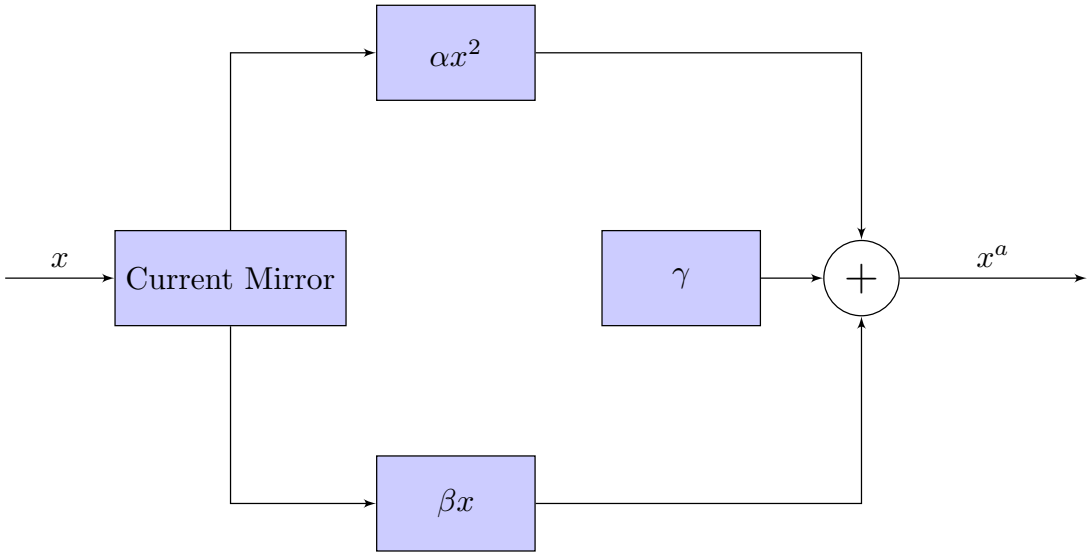


Figure 3.1: Proposed structure for implementing second order polynomial approximation.

3.1 Squaring Circuit

To implement the second order polynomial function, a squaring circuit will be used. Translinear principle can implement the circuit with fewer number of transistors. Figure 3.2, comprises one translinear loop formed by transistors M1-M4 operating in the saturation region.

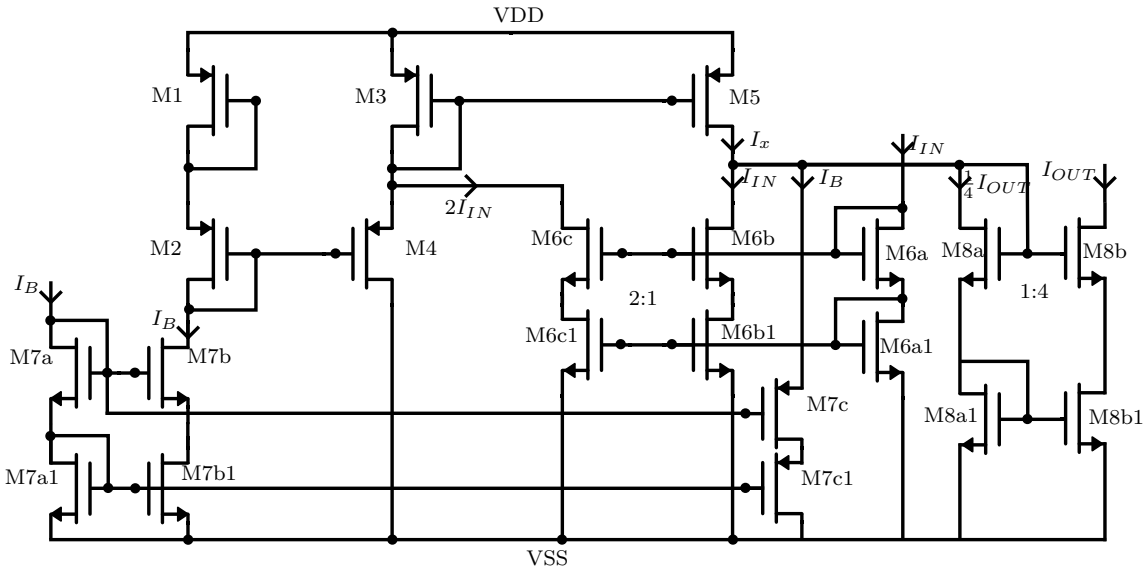


Figure 3.2: Squaring circuit based on translinear principle modified from [27].

Applying KVL to the translinear loop yields the following:

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} \tag{3.3}$$

Using the assumption that the transistors are well-matched and the transconductance values are equal,

$$\sqrt{I_{DS1}} + \sqrt{I_{DS2}} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} \tag{3.4}$$

The drain current of M1 and M2 will be equal, then the equation will become:

$$2\sqrt{I_B} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} \tag{3.5}$$

The drain current of M1 and M2 will be equal to bias current, I_B. The drain current of M3 will be mirrored to M5. This current will be equal to the sum of I_{IN}, I_B, and $\frac{1}{4}I_{OUT}$.

Let,

$$I_x = I_B + \frac{1}{4} I_{OUT} \tag{3.6}$$

Hence,

$$I_{DS3} = I_x + I_{IN} \tag{3.7}$$

and,

$$I_{DS5} = I_x - I_{IN} \tag{3.8}$$

Then, by substituting the value of I_{DS3} and I_{DS4} from equation (3.7)-(3.8) to equation (3.5),

$$2\sqrt{(I_B)} = \sqrt{(I_x + I_{IN})} + \sqrt{(I_x - I_{IN})} \tag{3.9}$$

By squaring each side, equation (3.9) reduces to:

$$4I_B - 2I_x = 2\sqrt{(I_x^2 - I_{IN}^2)} \tag{3.10}$$

By squaring again each side, equation (3.10) will reduce to:

$$I_x = \frac{I_{IN}^2}{4I_B} + I_B \tag{3.11}$$

By substituting I_x back from equation (3.6) to equation (3.11) and rearranging it, equation (3.11) becomes:

$$I_{OUT} = \frac{I_{IN}^2}{I_B} \tag{3.12}$$

Inspecting equation (3.12) shows that the output current will be proportional to the square of the input current normalized to the bias current.

Generally, the bulk connection of the transistors is connected to VDD for PMOS and GND for NMOS. However, in order to eliminate the Body Effect for the translinear loop, the bulk of M2 and M4 is connected to their source port hence $V_{SB} = 0$.

3.2 Coefficients of the approximated function

The MATLAB curve fitting tool was used to obtain the value of the coefficients α, β and γ of equation (3.2). Table 3.1 shows the value for several rational power functions from 0 to 4.

Table 3.1: Values of coefficient α, β, and γ of equation (3.2) for different rational power.

Power	0.10	0.19	0.63	0.90	1.39	1.50	1.75	1.91
α	-0.2267	-0.2453	-0.2942	-0.0971	0.4271	0.5474	0.7966	0.9314
β	0.4518	0.6060	1.1380	1.0700	0.6093	0.4868	0.2234	0.0764
γ	0.7638	0.6333	0.1497	0.0248	-0.0298	-0.0268	-0.0139	-0.0051
RMSE	0.0270	0.0452	0.0038	0.0042	0.0053	0.0054	0.0033	0.0013
Power	2.19	2.53	2.83	3.00	3.11	3.47	3.93	4.00
α	1.1300	1.3130	1.4410	1.500	1.5340	1.6250	1.7050	1.7140
β	-0.1476	-0.3639	-0.5227	-0.6000	-0.6456	-0.7739	-0.8985	-0.9143
γ	0.0108	0.0275	0.0423	0.05	0.0548	0.0689	0.0837	0.0857
RMSE	0.0031	0.0094	0.0168	0.0189	0.0211	0.0283	0.0369	0.0381

For α, the value will be negative for power function between 0 and 1. Then, it will increase by increasing the power until a reaches 4.00. Hence, the range of the value of α will be varied between -0.3 (for $a = 0.63$) and 1.72 (for $a = 4.00$). The value of β will be negative for a greater than 2. The range of β is between -0.92 (for $a = 4.00$) and 1.12 (for $a = 0.63$).

In this table, Root Mean Square Error (RMSE), as defined in equation (3.13), is used as one of the criteria to measure the goodness of the fitting function.

$$RMSE = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(M_i - C_i)^2} \tag{3.13}$$

M_i is the result from an approximation of rational power function and C_i is the reference of the ideal value of rational power function.

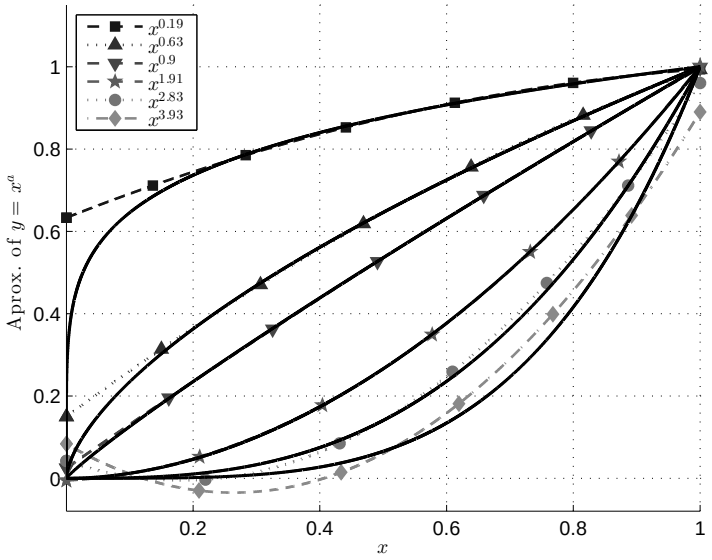


Figure 3.3: Approximation of some rational powered function from Table 3.1.

The best approximation occurs when the error is near to zero. Table 3.1 shows that the approximation performs is better when a is close to 1 and 2 (that is between $x^{0.63}$ and $x^{2.53}$) where the RMSE is less than 0.01.

A comparison between the exact calculation and the approximation of some powers is shown in Figure 3.3. The solid lines dedicated to the ideal rational powered function while the dashed lines show the approximated function. Figure 3.3 shows a big offset in the beginning of the approximated curve for lower value of a (e.g. $a = 0.19$). Plot of

Table 3.2: Values of coefficient α and β of equation (3.14) for different rational power.

Power	0.10	0.19	0.50	0.63	0.90	1.39	1.75	1.91
α	-2.7650	-2.3190	-1.1430	-0.7751	-0.1768	0.5241	0.8421	0.9480
β	3.5020	3.1090	2.0570	1.7220	1.1670	0.4919	0.1684	0.0563
RMSE	0.2398	0.1786	0.0606	0.0353	0.0058	0.0082	0.0050	0.0019
Power	2.15	2.53	2.83	3.00	3.11	3.47	3.93	4.00
α	1.0760	1.2200	1.3000	1.3330	1.3520	1.3960	1.4260	1.429
β	-0.0084	-0.2539	-0.3537	-0.4000	-0.4266	-0.4984	-0.5636	-0.5714
RMSE	0.0035	0.0132	0.0209	0.0252	0.0279	0.0364	0.0462	0.0476

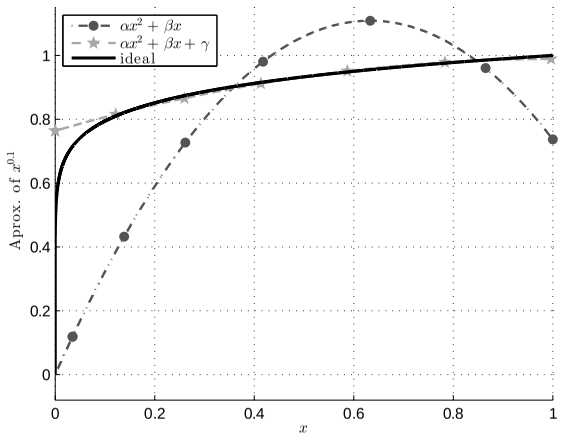
$x^{0.9}$ and $x^{1.91}$ shows the best approximation compared to other approximated curves. Plot of $x^{2.53}$ shows that the error is increasing but still provide a good approximation. But by raising a the error of the approximated curve increases significantly.

From Figure 3.3, it can be observed that there are huge zero offset problem in the approximation function of equation (3.2). Hence, another approximation will be introduced by setting γ is equal to 0. Thus, equation (3.2) will reduce to equation (3.14),

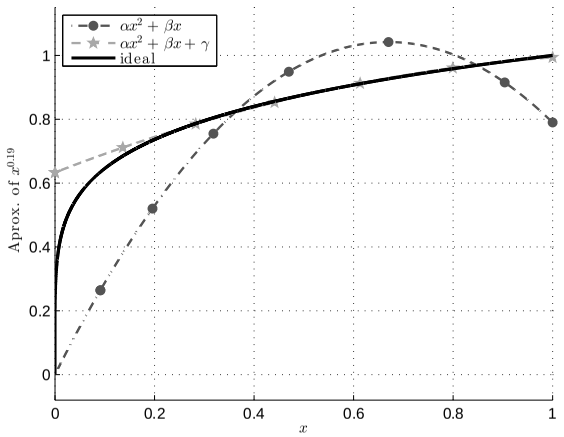
$$x^a \cong \alpha x^2 + \beta x \tag{3.14}$$

By using the same method, MATLAB curve fitting tool can be used to obtain the value of the new coefficients α and β for equation (3.14). The value of the coefficients α and β for some powers between 0 and 4 is compiled in Table 3.2. Figures 3.4 show the comparison of the rational power function approximated by equations (3.2), (3.14), and the ideal one. The dashed line with circle marker represents the approximation of rational power function by equation (3.14). The dash-dot line with star marker represents the approximation of rational power function by equation (3.2). In addition, the solid line is the reference of the ideal rational power function.

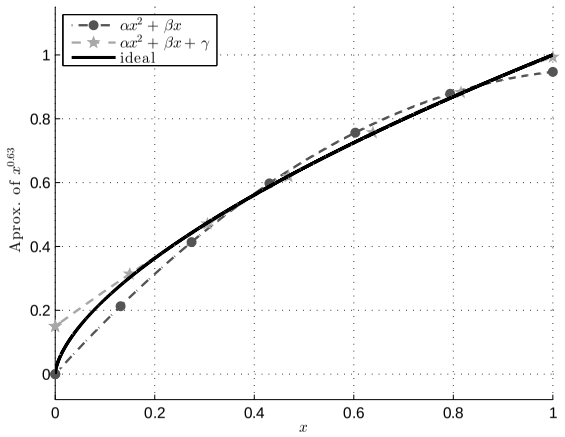
In reference of Figures 3.4, the new approximation of equation (3.14) suffers from the error for power lower than 0.63. But surprisingly, it shows good performance for higher power, especially for power between 0.63 and 2.15. In that range, the RMSE error of the new approximation of equation (3.14) is slightly higher than the approximation of equation (3.2). However, the approximation of equation (3.14) provides very small of zero offset and negative offset.



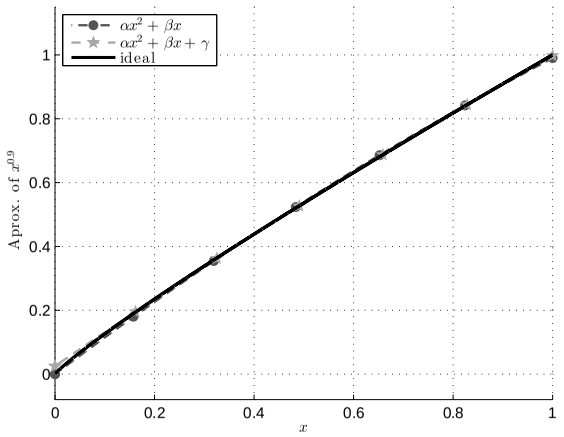
(a) $x^{0.10}$.



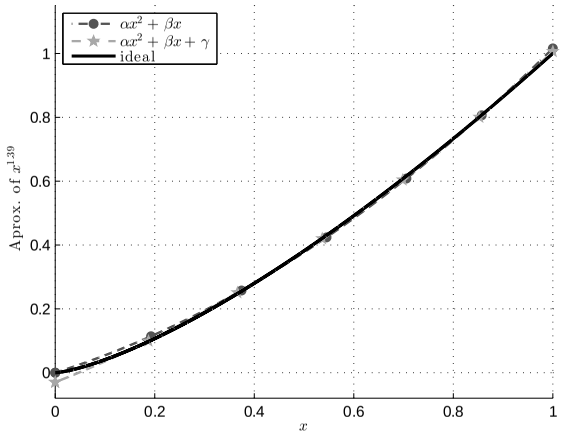
(b) $x^{0.19}$



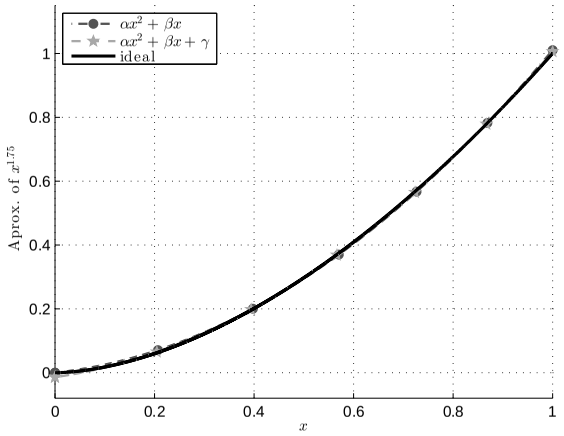
(c) $x^{0.63}$



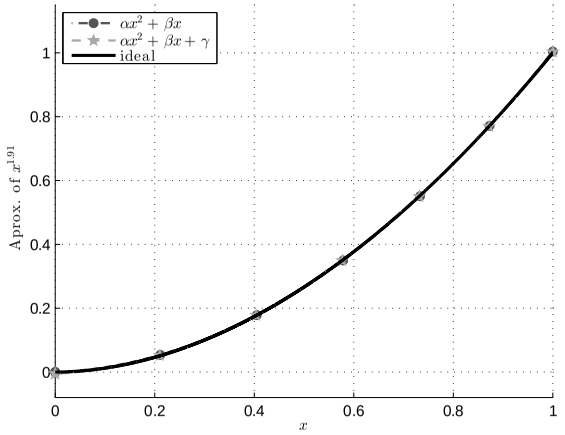
(d) $x^{0.90}$



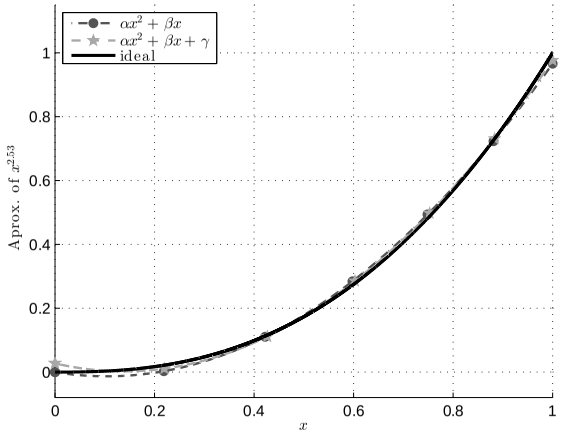
(e) $x^{1.39}$



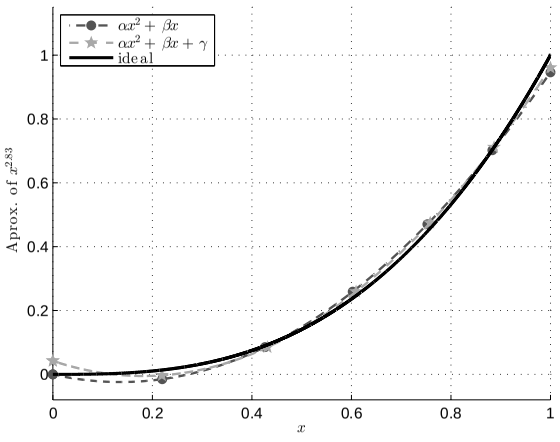
(f) $x^{1.75}$



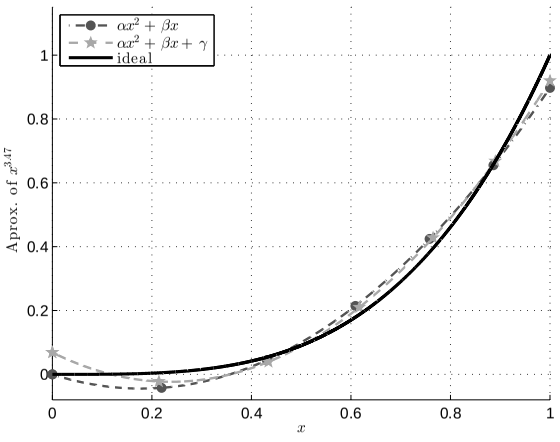
(g) $x^{1.91}$



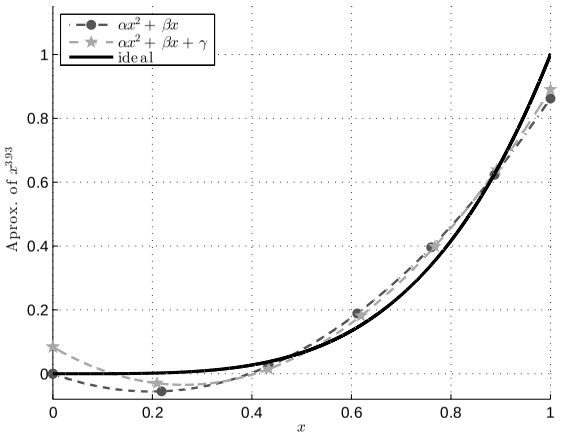
(h) $x^{2.53}$



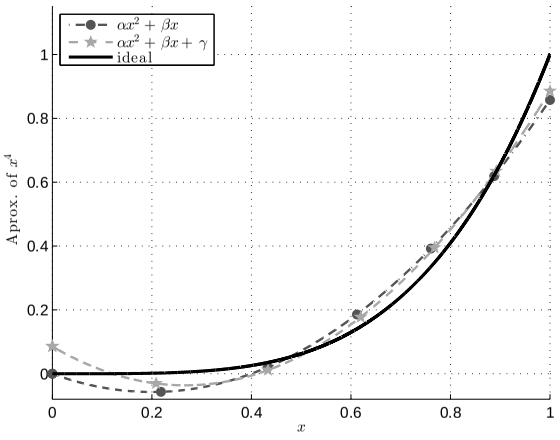
(i) $x^{2.83}$



(j) $x^{3.47}$



(k) $x^{3.93}$



(l) $x^{4.00}$

Figure 3.4: Comparison of two approximate function: second order polynomial with constant and without constant

3.3 Bidirectional Programmable Current Mirror

Programmable current mirror manages the value of the coefficients α and β. From Table 3.1, the range of α and β can be determined. For α, the maximum value is 1.72 and for β, the maximum value is 1.12. The sign of α and β should also be able to control either positive or negative. One of the splendid properties of current-mode circuits is that the currents can easily be added and the direction of flow of the current can be changed. One of the simplest methods to implement the programmable current mirror is by cascading several current mirrors and sum the current. The gain can be easily controlled by selecting which transistor should be on or off [8–10]. The circuit is shown in Figure 3.5. Cascode current mirror is used as it can perform better in terms of accuracy compared to the simple current mirror but remain simple to implement [28]. This method adapts the approach of the digital modes by switching the transistors, hence it can be easily implemented and controlled. But the downside of this approach- like most of the digital approaches- is that it will need very large size and the resolution is limited to the number of stacked transistors. The more digital codes, the better accuracy obtained. In this thesis, 8-bits programmable current mirror is selected. The maximum resolution is 1/128 which is an acceptable approximation to define α and β.

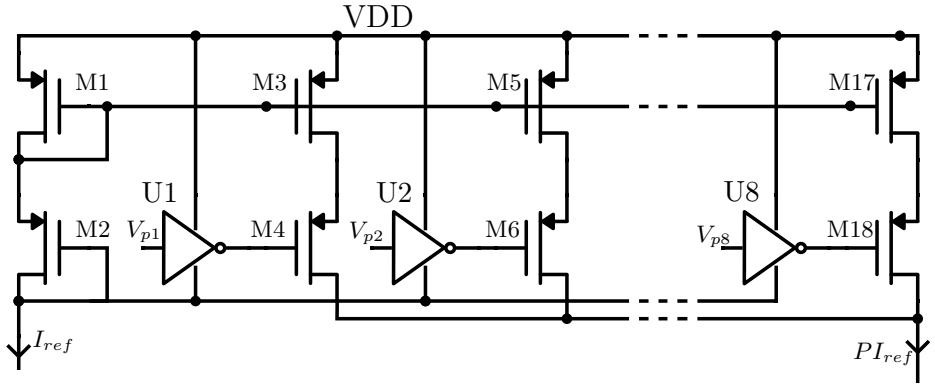


Figure 3.5: Cascode current mirror with selectable gain [8–10, 29].

Since the coefficients can be either positive or negative, the circuits need a current sign controller. Figure 3.6 shows a circuit to control the current flows by changing voltage V_{bi1} and V_{bi2}. V_{bi2} is always set as an invert of V_{bi1}.

To get the positive current flow, PMOS transistors M7 - M9 should be active, while NMOS transistor M5 is set to be off. Hence, V_{bi1} is set to 0 and V_{bi2} is set to 1. Vice versa, to get the negative current flow, NMOS transistor M5 should be on, and the PMOS transistors M7 - M9 are should be off. Hence, V_{bi1} is set to 1 and V_{bi2} is set to 0.

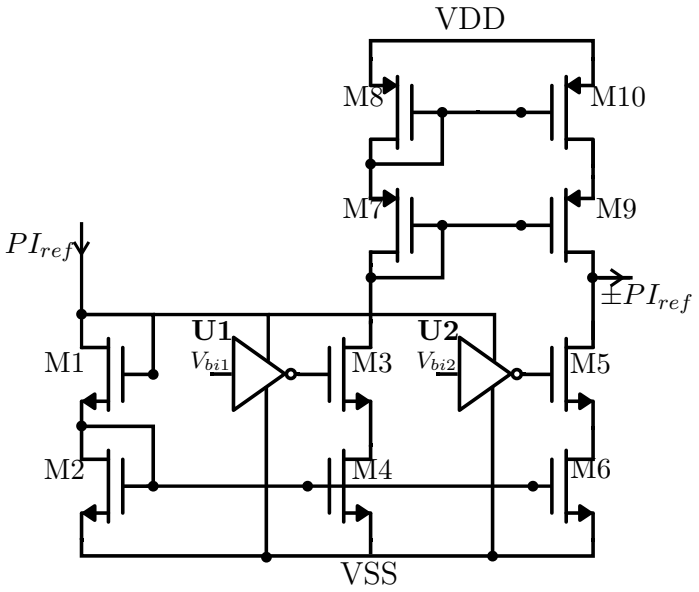


Figure 3.6: Current mirror sign controller.

Table 3.3 shows bit configuration for different value of α and β based on Table 3.1. The relative error shown in the tables is relatively small.

Table 3.3: Bit configuration for different values of α and β of equation (3.2).

Power	Required Value	Vbi1	Vb1	Vb2	Vb3	Vb4	Vb5	Vb6	Vb7	Vb8	Obtained Value	Relative Error
			$\frac{3}{4}$	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	$\frac{1}{32}$	$\frac{1}{64}$	$\frac{1}{128}$		
0.19	-0.2453	1	0	0	0	1	1	1	1	1	-0.242188	1%
	0.6060	0	0	1	0	0	1	1	1	0	0.609375	1%
0.63	-0.2942	1	0	0	1	0	0	1	1	0	-0.296875	1%
	1.1380	0	1	0	1	1	0	0	1	0	1.140625	0%
0.90	-0.0971	1	0	0	0	0	1	1	0	0	-0.09375	3%
	1.0700	0	1	0	1	0	1	0	0	1	1.0703125	0%
1.39	0.4271	0	0	0	1	1	0	1	1	1	0.4296875	1%
	0.6093	0	0	1	0	0	1	1	1	0	0.609375	0%
1.75	0.7966	0	1	0	0	0	0	1	1	0	0.796875	0%
	0.2234	0	0	0	0	1	1	1	0	1	0.2265625	1%
1.91	0.9314	0	1	0	0	1	0	1	1	1	0.9296875	0%
	0.0764	0	0	0	0	0	1	0	1	0	0.078125	2%
2.53	1.3130	0	1	1	0	0	1	0	0	0	1.3125	0%
	-0.3639	1	0	0	1	0	1	1	1	1	-0.367188	1%
2.83	1.4410	0	1	1	0	1	1	0	0	0	1.4375	0%
	-0.5227	1	0	1	0	0	0	0	1	1	-0.523438	0%
3.00	1.5000	0	1	1	1	0	0	0	0	0	1.5	0%
	-0.6000	1	0	1	0	0	1	1	0	1	-0.601563	0%
3.47	1.6250	0	1	1	1	1	0	0	0	0	1.625	0%
	-0.7739	1	1	0	0	0	0	0	1	1	-0.773438	0%
3.93	1.7050	0	1	1	1	1	1	0	1	0	1.703125	0%
	-0.8985	1	1	0	0	1	0	0	1	1	-0.898438	0%
4.00	1.7140	0	1	1	1	1	1	0	1	1	1.7109375	0%
	-0.9143	1	1	0	0	1	0	1	0	1	-0.914063	0%

Table 3.4: Bit configuration for different value of α and β of equation (3.14).

Power	Required Value	Vbi3	Vb1	Vb2	Vb3	Vb4	Vb5	Vb6	Vb7	Vb8	Obtained Value	Relative Error
			$\frac{3}{4}$	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	$\frac{1}{32}$	$\frac{1}{64}$	$\frac{1}{128}$		
0.63	-0.7751	1	1	0	0	0	0	0	1	1	-0.7734375	0%
	1.7220	0	1	1	1	1	1	1	0	0	1.71875	0%
0.90	-0.1768	1	0	0	0	1	0	1	1	1	-0.1796875	2%
	1.1670	0	1	0	1	1	0	1	0	1	1.1640625	0%
1.39	0.5241	0	0	1	0	0	0	0	1	1	0.5234375	0%
	0.4919	0	0	0	1	1	1	1	1	1	0.4921875	0%
1.75	0.8421	0	1	0	0	0	1	0	1	1	0.8359375	1%
	0.1684	0	0	0	0	1	0	1	0	1	0.1640625	3%
1.91	0.9480	0	1	0	0	1	1	0	0	1	0.9453125	0%
	0.0563	0	0	0	0	0	0	1	1	1	0.0546875	3%
2.15	0.9940	0	1	0	0	1	1	1	1	1	0.9921875	0%
	-0.0139	1	0	0	0	0	0	0	1	0	-0.015625	13%
2.53	1.2200	0	1	0	1	1	1	1	0	0	1.21875	0%
	-0.2539	1	0	0	1	0	0	0	0	0	-0.25	2%
2.83	1.3000	0	1	1	0	0	0	1	1	0	1.296875	0%
	-0.3537	1	0	0	1	0	1	1	0	1	-0.3515625	1%
3.11	1.3520	0	1	1	0	0	1	1	0	1	1.3515625	0%
	-0.4266	1	0	0	1	1	0	1	1	1	-0.4296875	1%
3.47	1.3960	0	1	1	0	1	0	0	1	1	1.3984375	0%
	-0.4984	1	0	0	1	1	1	1	1	1	-0.4921875	1%
3.93	1.4260	0	1	1	0	1	0	1	1	1	1.4296875	0%
	-0.5636	1	0	1	0	0	1	0	0	0	-0.5625	0%
4.00	1.4290	0	1	1	0	1	0	1	1	1	1.4296875	0%
	-0.5714	1	0	1	0	0	1	0	0	1	-0.5703125	0%

CHAPTER 4

SIMULATION RESULTS

T-Spice with library BSIM3v3 TSMC CMOS RF 180 nm is used to simulate the circuit and verify the design. Dual power supply voltage is set as $VDD = -VSS = 1.25V$. Input current is swept from 0 to 10μA. Aspect ratio (W/L) of the transistors used in the circuit are shown in Tables 4.1-4.4. The simulation results are normalized to the bias current $I_B = 10\mu A$. The gray dash-dot line with marker circle is the simulation result from T-SPICE and the black solid line is the ideal result. Temperature is set under normal temperature 25 °C

Table 4.1: Aspect ratios of transistors used in the squaring unit of Figure 3.2

Transistor	W/L ($\mu m/\mu m$)	Transistor	W/L ($\mu m/\mu m$)
M1-M2	20/4.75	M7a-M7a1	2/0.8
M3-M4	20/4.78	M7b-M7b1	2/0.81
M5	20/4.72	M7c-M7c1	2/0.78
M6a-M6a1	2/0.8	M8a-M8a1	2/0.8
M6b-M6b1	2/0.8	M8b-M8b1	8/0.8
M6c-M6c1	4/0.8		

Table 4.2: Aspect ratios of transistors used in the inverter of Figure 3.5 and 3.6

Transistor	W/L ($\mu m/\mu m$)
PMOS	1.125/0.25
NMOS	0.375/0.25

Table 4.3: Aspect ratios of transistors used in the programmable current mirror of Figure 3.5 for coefficient α and β

Transistor	W/L ($\mu m/\mu m$)	Ratio Output Current
M1-M2 (Reference)	64/0.25	1
M3-M4	48/0.25	0.75
M5-M6	32/0.25	0.50
M7-M8	16/0.25	0.25
M9-M10	8/0.25	0.125
M11-M12	4/0.25	0.0625
M13-M14	2/0.25	0.031250
M15-M16	1/0.25	0.015625
M17-M18	0.5/0.25	0.0078125

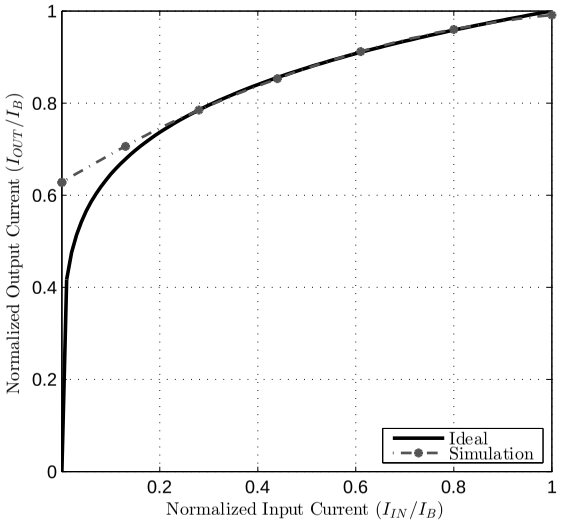
Table 4.4: Aspect ratios of transistors used in bidirectional current sign inverter of Figure 3.6

Transistor	W/L ($\mu m/\mu m$)
M1-M10	3/0.5

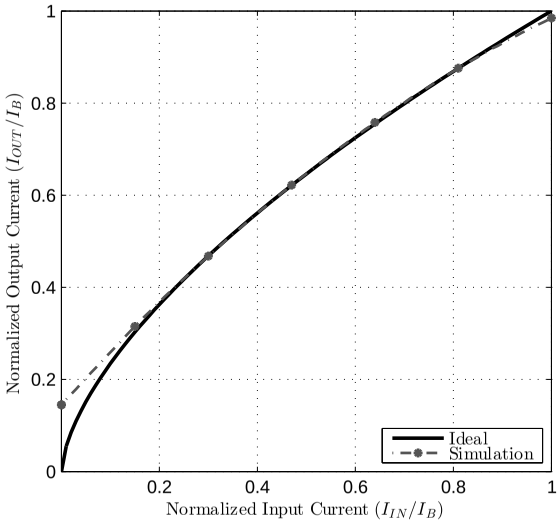
4.1 Second Order Polynomial Approximation

The simulation results of rational powered function generator based on Equation (3.2) is depicted in Figures 4.1. Generally, the results are in agreement with the MATLAB model (Figures 3.4). There is huge zero offset in the normalized output of about 0.63 for lower power ($a = 0.19$) as shown in Figure 4.1a. By increasing the power $a = 0.63$, (Figure 4.1b), the offset is gradually decreasing until it becomes 0.021 for $a = 0.9$ (Figure 4.1c). For lower power like 0.19 and 0.63, the error can significantly be reduced by limiting the normalized input to be more than 0.2. The good performance of the approximation of Equation (3.2) is continued to $a = 1.39$ (Figure 4.1d) and $a = 1.91$ (Figure 4.1e). When the power is increasing to 2.53 (Figure 4.1f), the zero offset about 0.1 remain occurs. By increasing the power to $a = 3.00$ (Figure 4.1g), the zero offset is reduced to 0.07, but then the result shows the negative offset of 0.03. This can not be accepted. To overcome this, the normalized input may be limited to be more than 0.38. The error and the negative offset rose gradually until it reaches to 0.06 at $a = 4.00$ (Figure 4.1h). By limiting the normalized input to 0.45 will help to overcome the negative offset. There is also a negative offset of 0.023 for power 1.39 (Figure 4.1d). By limiting the input to be greater than 0.05, the negative offset can be avoided.

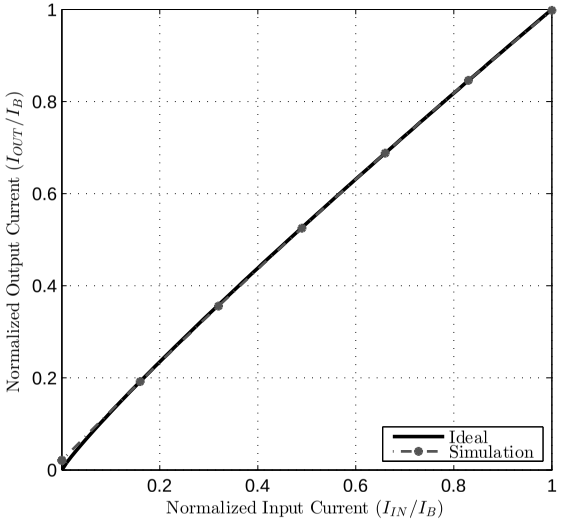
The root means square error (RMSE) of some rational power functions approximated by Equation (3.2) is compiled in Table 4.5. The largest error is about 7%. Then RMSE fell gradually by increasing the power to 0.90 by RMSE below 0.5%. The error then steadily rose until $a = 1.91$. But then the error dramatically increased for power more than 2.53. It can be concluded from Table 4.5, that the approximation of rational function power by using Equation (3.2), in terms of RMSE, has better performance if the power is restricted to be in the range of power of 0.63 until 3.00.



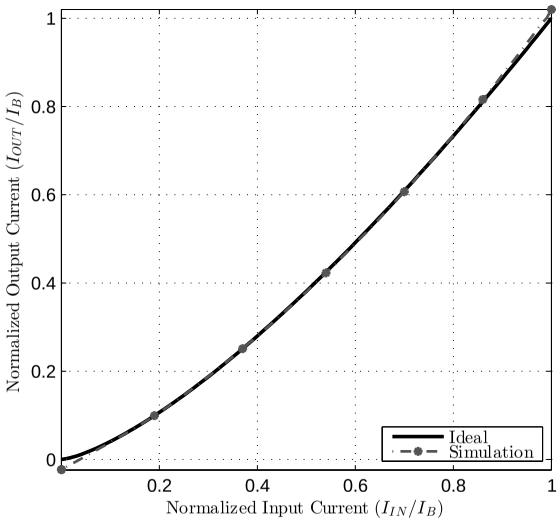
(a) $x^{0.19}$



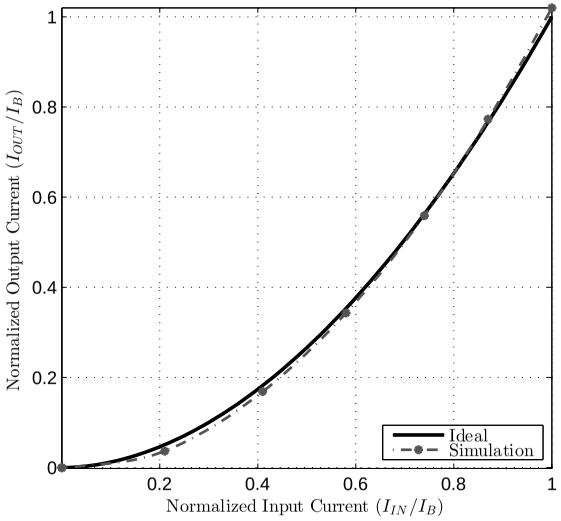
(b) $x^{0.63}$



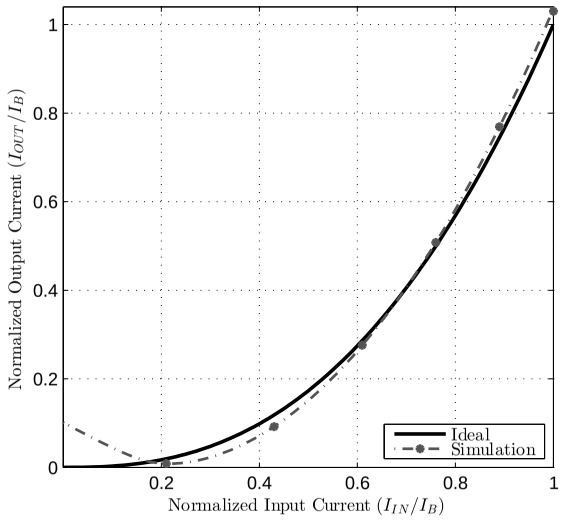
(c) $x^{0.9}$



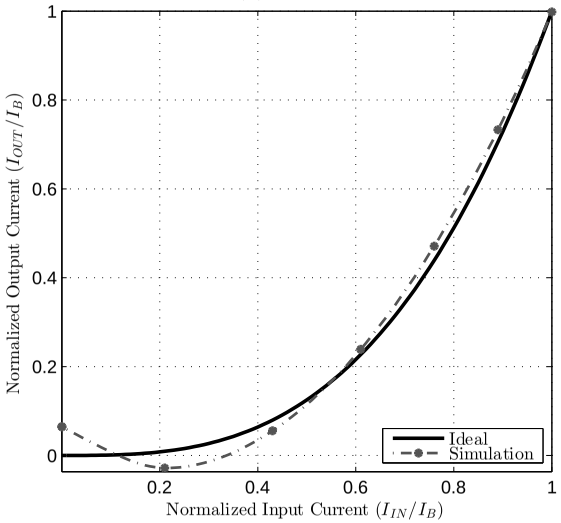
(d) $x^{1.39}$



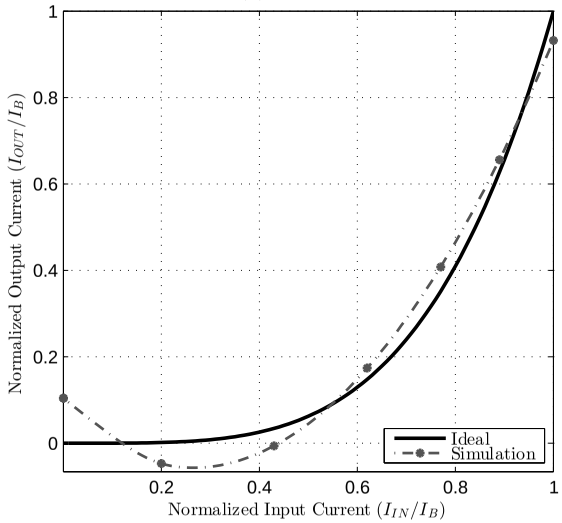
(e) $x^{1.91}$



(f) $x^{2.53}$



(g) $x^{3.00}$



(h) $x^{4.00}$

Figure 4.1: Simulation result of second order polynomial

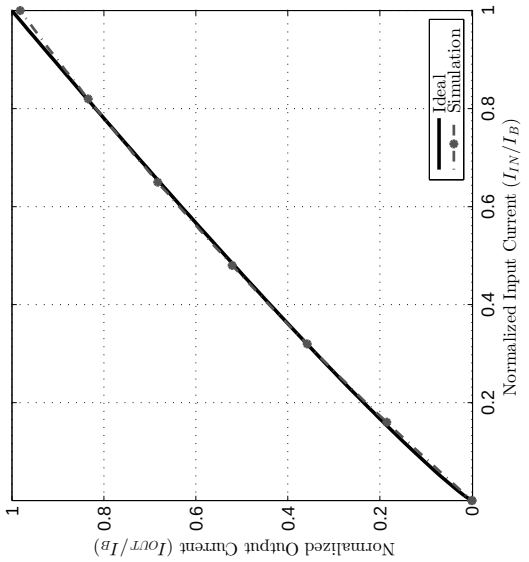
Table 4.5: The RMSE of simulation result of second order polynomial approximation for some rational power.

Power	RMSE
0.19	7.26%
0.63	2.40%
0.90	0.37%
1.39	0.60%
1.91	1.06%
2.53	3.12%
3.00	2.85%
4.00	4.57%

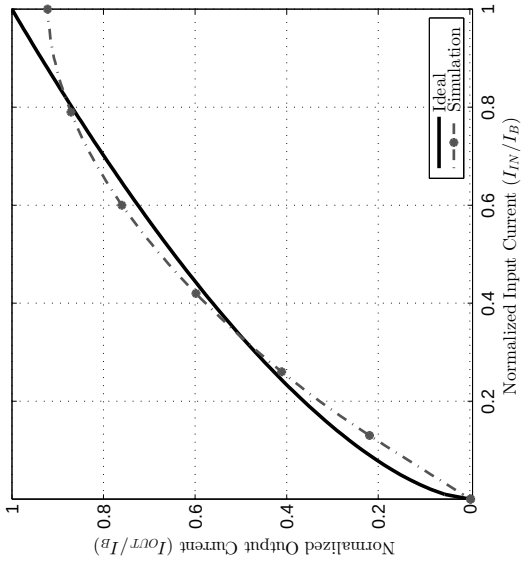
4.2 Second Order Polynomial Approximation without Constant

In this section, some simulation results based on the approximation of Equation (3.14) is presented in Figures 4.2.

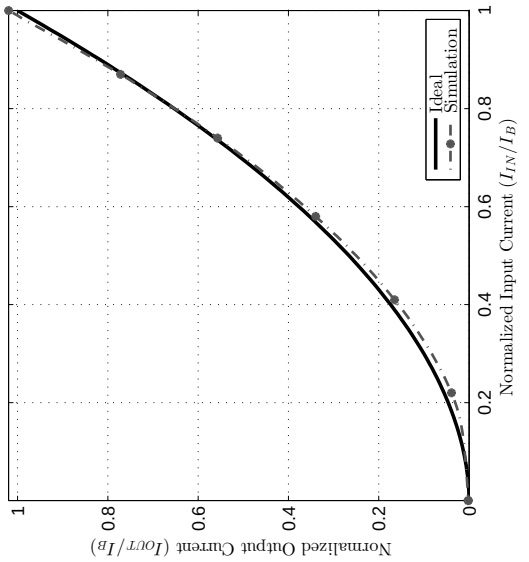
By setting the DC constant current of γ, can be expected zero offset. However, there is a very small zero offset due to non-ideality of the circuit, especially the squaring circuit. For the power of 0.63 (Figure 4.2a), there is a big error spreading around the curve. As shown in MATLAB model in Figure 3.4, by decreasing the power to 0, the performance of this approximation is very poor. However, by increasing the power, the error is reduced. This approximation has the best performance for $a = 0.90$ (Figure 4.2b). Then, the error gradually increased by increasing the power (Figure 4.2a to 4.2f). When the power reaches 2.15, it starts to show negative offset. The negative offset can be trimmed by limiting the normalized input to the range of 0.2-1.0. The negative offset keep increasing in Figure 4.2f for power 2.53. To overcome this problem, the normalized input should be limited to the range of 0.3-1.0.



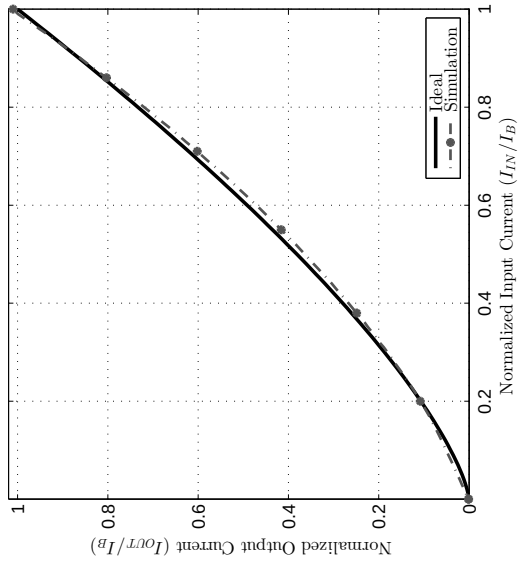
(a) $x^{0.63}$



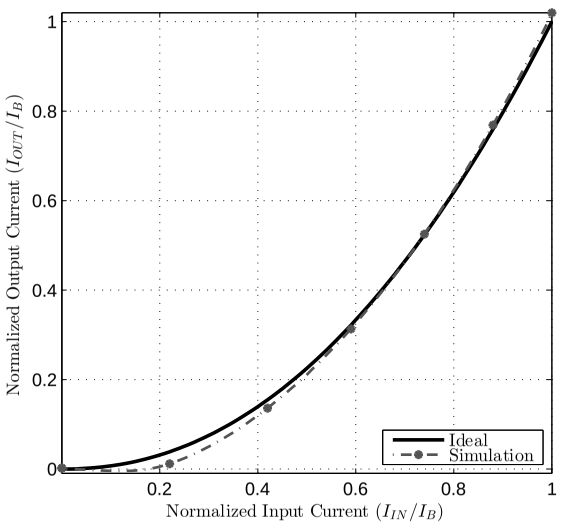
(b) $x^{0.9}$



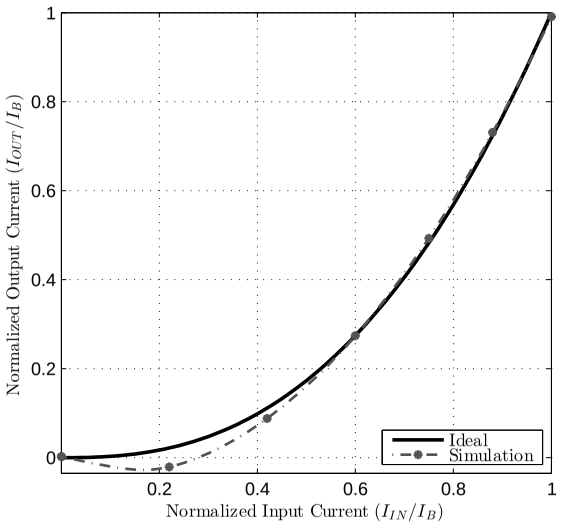
(c) $x^{1.39}$



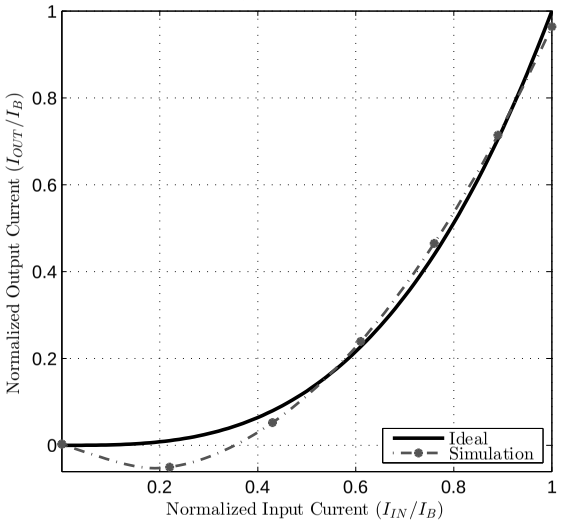
(d) $x^{1.91}$



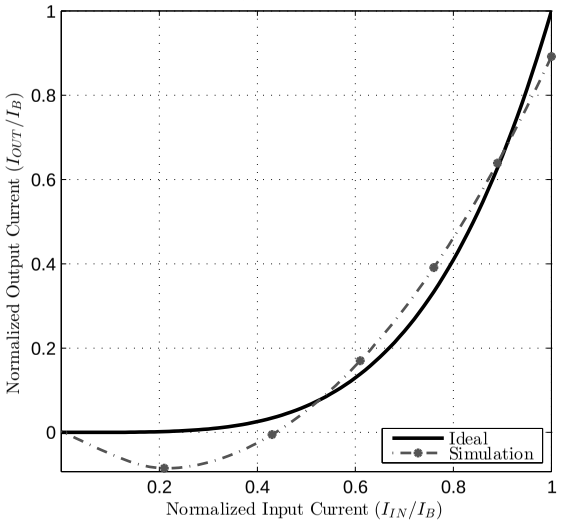
(e) $x^{2.15}$



(f) $x^{2.53}$



(g) $x^{3.00}$



(h) $x^{4.00}$

Figure 4.2: Simulation result of second order polynomial approximation without constant

Table 4.6: The RMSE of simulation result of second order approximation without constant for some rational power.

Power	RMSE
0.63	3.65%
0.90	0.64%
1.39	1.29%
1.91	1.28%
2.15	1.53%
2.53	2.17%
3.00	3.26%
4.00	5.38%

The root means square error (RMSE) of some rational power approximated of Equation (3.14) is compiled in Table 4.6. Compared to Table 4.5, this approximation has more limited range of the power and has slightly larger RMSE except for power 2.53. However, the approximation of Equation (3.14) offers simpler approach without needing to inject constant DC current which means less power consumption. Moreover, the zero offset can also be significantly reduced to be very near to zero. It means that when the input is 0, there will be no current flowing in the output port.

4.3 Mismatch Analysis

4.3.1 Temperature Sweep

In this section, simulation for temperature analysis is carried out. Temperature is varied from $-25\,^{\circ}\mathrm{C}$ to $75\,^{\circ}\mathrm{C}$ with step of $25\,^{\circ}\mathrm{C}$. The results are shown in Figures 4.3 to 4.4. The black solid line is the ideal result as the reference, while the others grayish dashed and doted lines are from the simulation results. Different markers show different temperature. The circle, the square, the diamond, the upward-pointing triangle, and the downward-pointing triangle are respectively shown the temperature of $-25\,^{\circ}\mathrm{C}$, 0,

25 °C, 50 °C, and 75 °C. The percentage of RMSE of temperature sweep is compiled in Table 4.7 (approximation based on Equation (3.2)) and Table 4.8 (approximation based on Equation (3.14)). The range is the width from the maximum RMSE to the minimum one. Bigger range could be a sign that the circuit suffers from temperature change and vice versa, smaller range could be a sign that the circuit has more sustainable during temperature changes.

Table 4.7: The RMSE of temperature sweep of second order polynomial approximation.

Power	RMSE					
	−25 °C	0	25 °C	50 °C	75 °C	Range
0.19	7.27%	7.27%	7.26%	7.24%	7.22%	0.05%
0.63	2.43%	2.41%	2.40%	2.37%	2.33%	0.10%
0.90	0.37%	0.37%	0.37%	0.36%	0.36%	0.01%
1.39	0.59%	0.60%	0.60%	0.61%	0.61%	0.02%
1.91	1.38%	1.20%	1.06%	0.91%	0.78%	0.60%
2.53	3.18%	3.13%	3.12%	3.16%	3.25%	0.13%
3.00	2.97%	2.91%	2.85%	2.77%	2.69%	0.28%
4.00	4.71%	4.64%	4.57%	4.49%	4.43%	0.28%

The temperature sweep test reveals that the circuit for both approximation has a good performance in the range −25 °C to 75 °C. Especially for lower power, $a \leq 1.39$, the variations are almost unnoticeable. The percentage of RMSE only increases by less than 0.5% compared to the performance of Figures 4.3 and 4.4 at 25 °C. For power 4, by using approximation of equation (3.14), RMSE at −25 °C is 5.68%, increasing about 0.3% compared to the performance of Figure 4.4h at 25 °C (5.38%). In approximation of equation (3.2), for power 1.91, RMSE at −25 °C is 1.38% compared to the performance of Figure 4.3e of 1.06% at 25 °C. The best performance for both approximations is at power 0.9, the RMSE of the approximation of equation (3.2) only increases by 0.1% compared to the performance of Figure 4.3b at 25 °C while for approximation of equation (3.14),

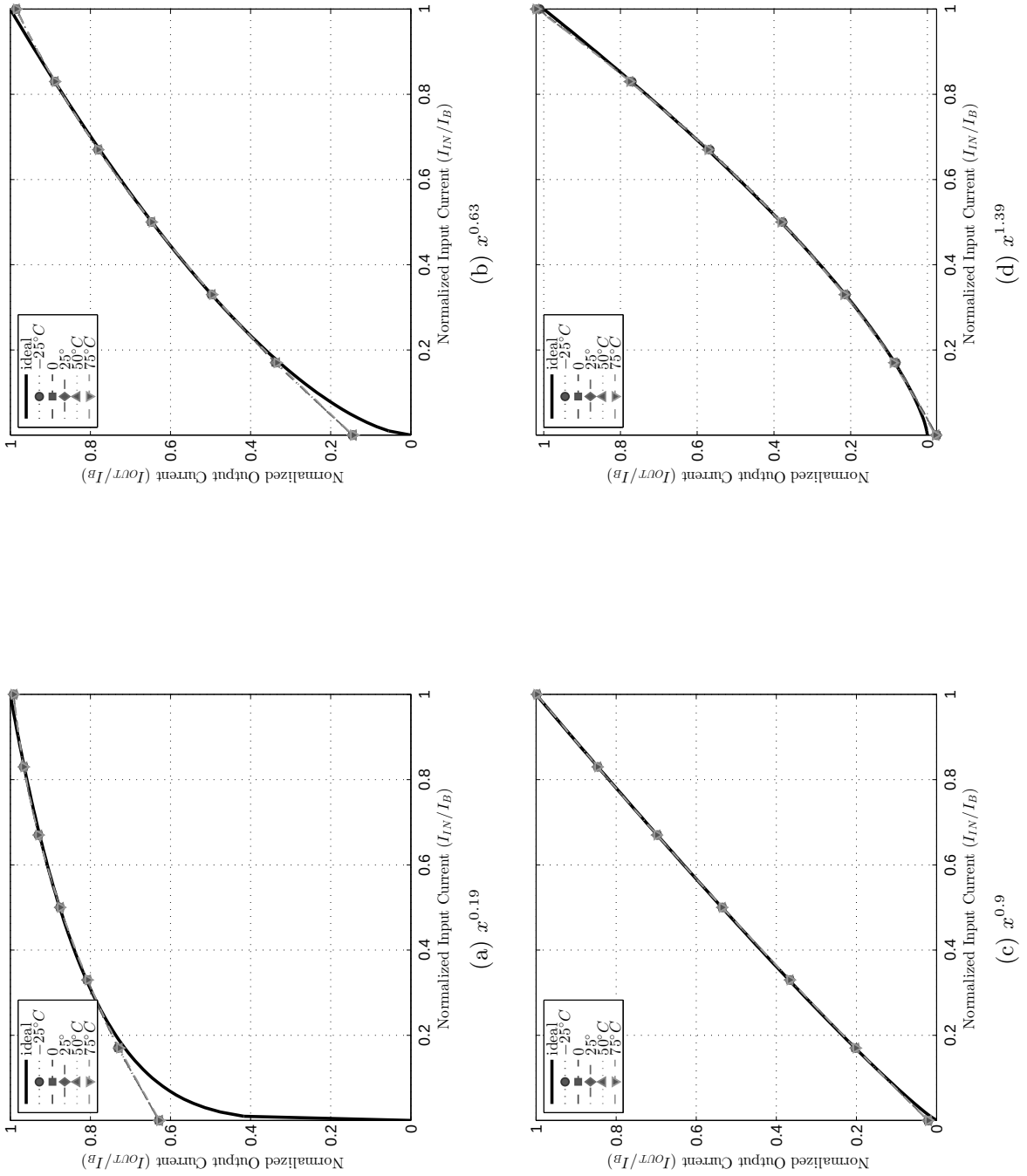
it increases by 0.4%, compared to the performance of Figure 4.4b at 25 °C. The spread of the range on Table 4.7 and Table 4.8 indicates that generally, during temperature sweep, the performance of the approximation of equation (3.2) is slightly better than the approximation of equation (3.14).

Table 4.8: The RMSE of temperature sweep of second order polynomial approximation without constant.

Power	RMSE					
	−25 °C	0	25 °C	50 °C	75 °C	Range
0.63	3.60%	3.61%	3.65%	3.70%	3.80%	0.20%
0.90	0.64%	0.64%	0.64%	0.66%	0.68%	0.04%
1.39	1.55%	1.39%	1.29%	1.25%	1.23%	0.32%
1.91	1.63%	1.44%	1.28%	1.13%	0.99%	0.64%
2.15	1.86%	1.69%	1.53%	1.33%	1.11%	0.75%
2.53	2.57%	2.37%	2.17%	1.94%	1.67%	0.90%
3.00	3.61%	3.44%	3.26%	3.03%	2.77%	0.84%
4.00	5.68%	5.54%	5.38%	5.18%	4.94%	0.74%

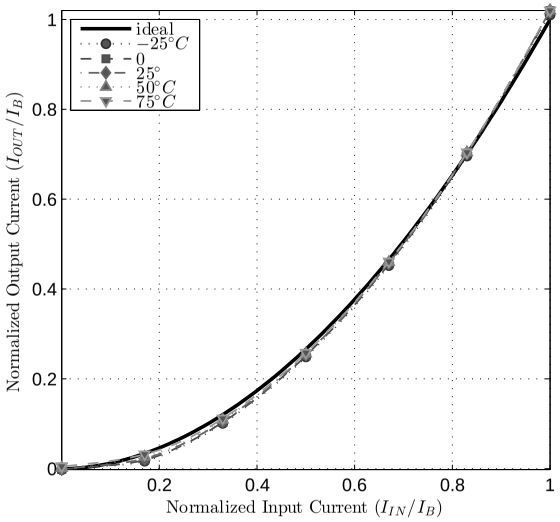
4.3.2 Monte Carlo Analysis

In the simulation results reported in Figures 4.1a and 4.2h, the transistors are assumed to be perfectly matched. However, practically there are many parameters that could affect the mismatch. To investigate the effect of parameter mismatches, several mismatch analysis will be performed using Monte Carlo simulation by varying the transistors size, the threshold voltage (Vth0), and the gate-oxide thickness (tox) parameters using Gaussian Distribution relatively about 3% with 100 samples. As a comparison, Monte Carlo simulation by using built-in statistical parameter data from the library TSMC RF 180nm will also be performed.

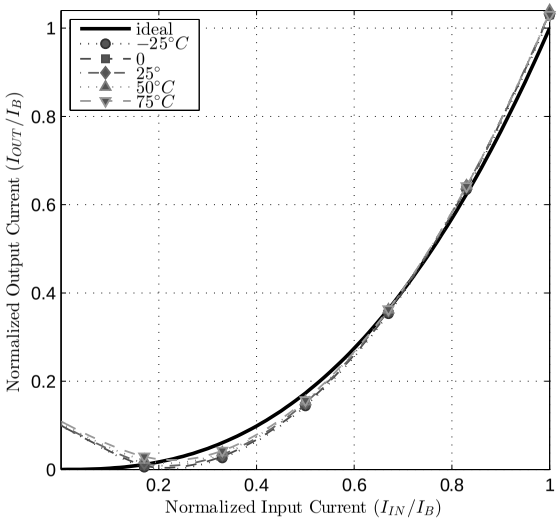


(a) $x^{0.19}$ (b) $x^{0.63}$

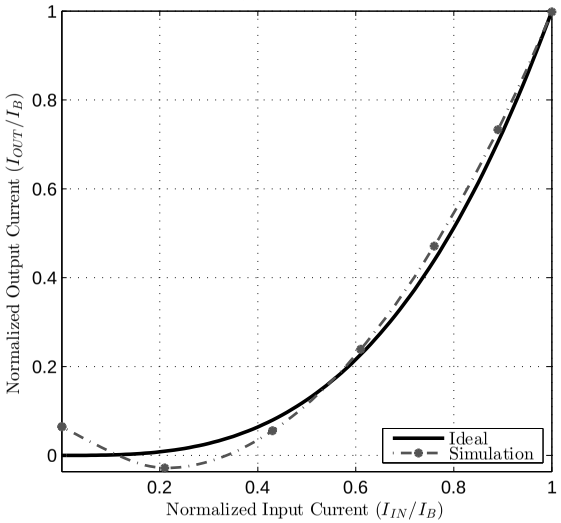
(c) $x^{0.9}$ (d) $x^{1.39}$



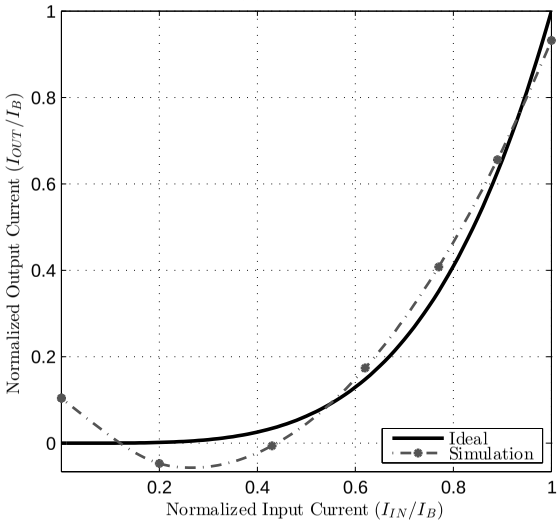
(e) $x^{1.91}$



(f) $x^{2.53}$

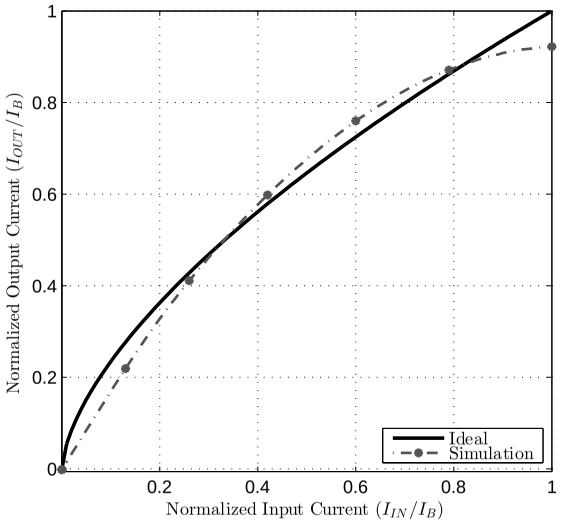


(g) $x^{3.00}$

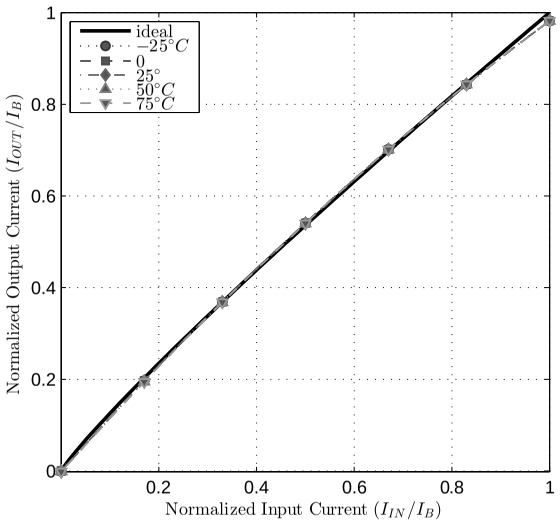


(h) $x^{4.00}$

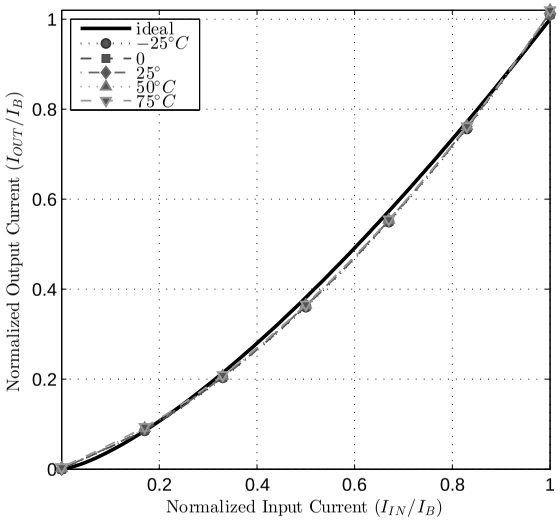
Figure 4.3: Temperature sweep of second order polynomial approximation.



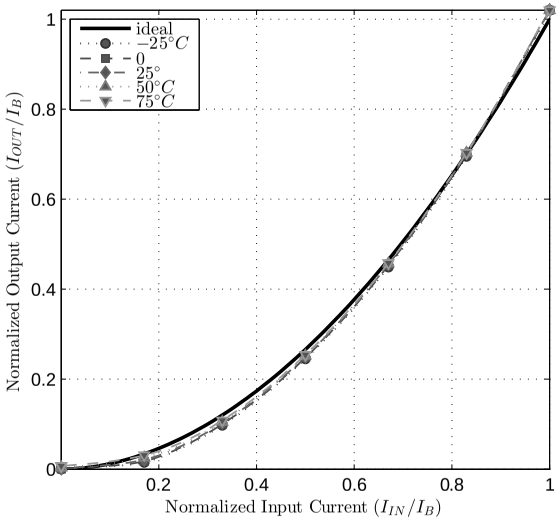
(a) $x^{0.63}$



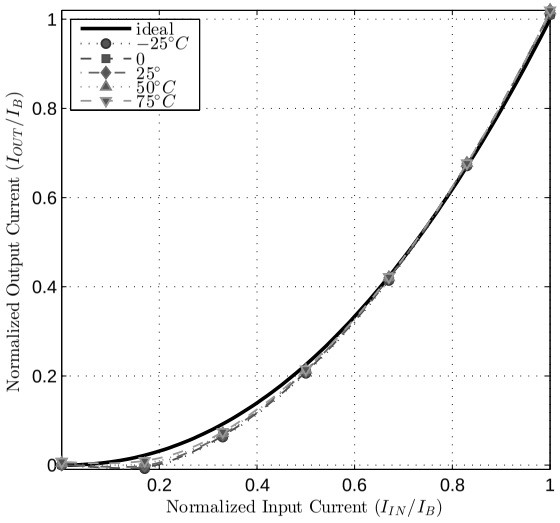
(b) $x^{0.9}$



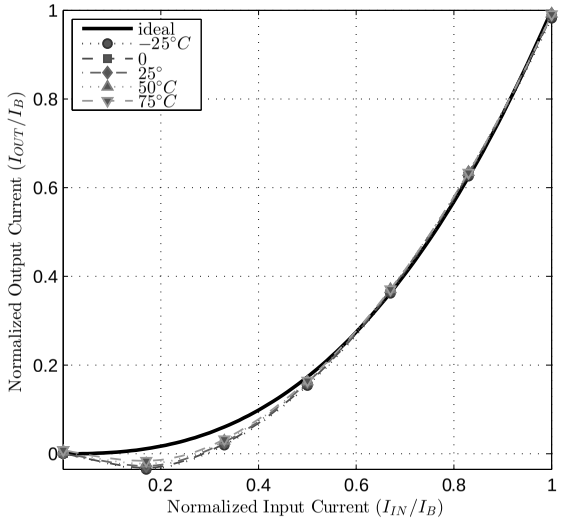
(c) $x^{1.39}$



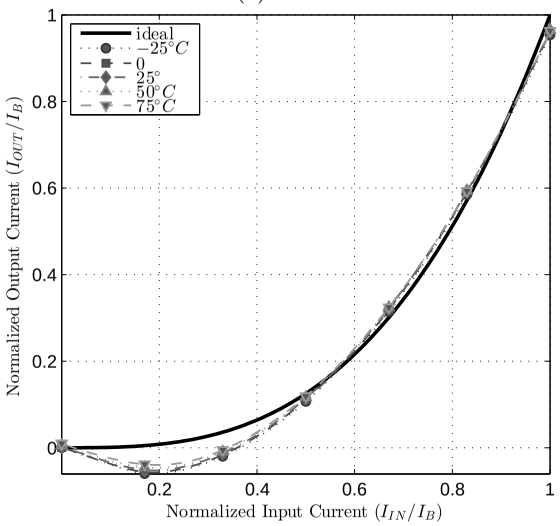
(d) $x^{1.91}$



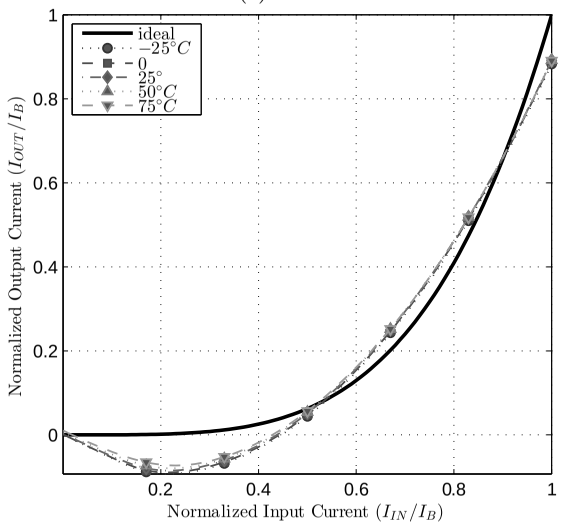
(e) $x^{2.15}$



(f) $x^{2.53}$



(g) $x^{3.00}$



(h) $x^{4.00}$

Figure 4.4: Temperature sweep of second order polynomial approximation without constant

Monte Carlo simulation by varying size ratio

In this section, Monte Carlo simulation by varying the size of all the transistors by Gaussian distribution 3% will be performed. The results of the simulation are depicted in Figure 4.5 and 4.6. The statistical data of Monte Carlo simulation by varying size of the transistors is presented on Tables 4.9 and 4.10. Typical column on Tables 4.9 and 4.10 shows the simulation results without mismatch condition as shown in Tables 4.5 and 4.6 for reference. StdDev column shows standard deviation value of the statistical data. Standard deviation tells us how close the RMSE of the samples to the mean RMSE. Higher value illustrates that the samples are more scattered far from the mean. Vice versa, lower value of standard deviation illustrates that the samples are more concentrated near to the mean. In other words, higher value of standard deviation indicates the circuit suffer from variations and lower standard deviation reveals the circuit is more sustainable from variations.

Table 4.9: Monte Carlo analysis with 3% transistor size variation of second order polynomial

Power	RMSE						
	Typical	Max	Min	Mean	Median	Range	StdDev
0.19	7.26%	7.26%	7.25%	7.26%	7.26%	0.01%	0.00%
0.63	2.40%	2.41%	2.40%	2.40%	2.40%	0.01%	0.00%
0.90	0.37%	0.38%	0.36%	0.37%	0.37%	0.02%	0.00%
1.39	0.60%	0.80%	0.53%	0.63%	0.61%	0.26%	0.06%
1.91	1.06%	1.34%	0.96%	1.06%	1.05%	0.38%	0.06%
2.53	3.12%	3.20%	3.00%	3.09%	3.08%	0.20%	0.04%
3.00	2.85%	3.00%	2.77%	2.86%	2.86%	0.23%	0.05%
4.00	4.57%	4.70%	4.50%	4.58%	4.58%	0.20%	0.03%

As shown in Tables 4.9 and 4.10, the lower power ($a < 1$) has the lowest error with standard deviation up to 0.01% and the range of the maximum and the minimum RMSE is lower 1%. The standard deviation is very small, lower than 0.1% of the error. Thus,

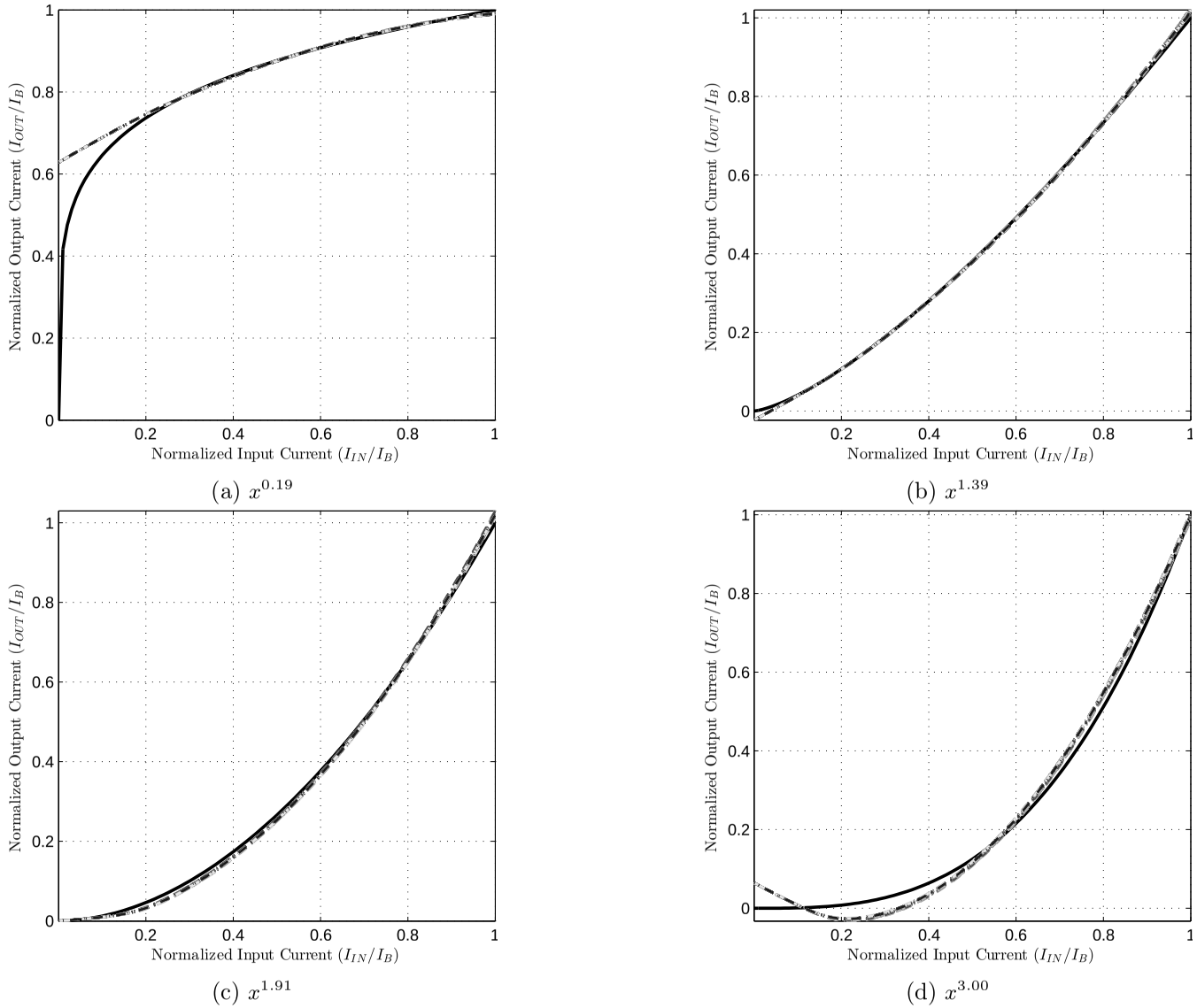
the proposed circuits for both approximations are only slightly affected by the variation of the size of the transistors.

Table 4.10: Monte Carlo analysis with 3% transistor size variation of second order polynomial without constant.

Power	RMSE						
	Typical	Max	Min	Mean	Median	Range	StdDev
0.63	3.65%	3.68%	3.64%	3.65%	3.65%	0.04%	0.01%
0.90	0.64%	0.68%	0.63%	0.66%	0.65%	0.06%	0.01%
1.39	1.29%	1.54%	1.08%	1.29%	1.27%	0.46%	0.09%
1.91	1.28%	1.58%	1.17%	1.32%	1.30%	0.40%	0.08%
2.15	1.53%	1.66%	1.45%	1.53%	1.53%	0.22%	0.05%
2.53	2.17%	2.39%	2.07%	2.18%	2.18%	0.32%	0.07%
3.00	3.26%	3.39%	3.16%	3.26%	3.26%	0.23%	0.05%
4.00	5.38%	5.54%	5.32%	5.38%	5.38%	0.23%	0.04%

Monte Carlo simulation by varying parameter *tox*

In this section, Monte Carlo simulation by varying parameter *tox* of all the transistors by Gaussian distribution around 3% will be performed. The results are depicted in Figures 4.7 and 4.8. The statistical data of Monte Carlo simulation by varying parameter *tox* of the transistors is presented on Tables 4.11 and 4.12. The proposed circuit is more sensitive to variations in the parameter *tox*. The worst case can be seen for power 1.39 in the approximation of equation (3.2) (Figure 4.7b) with standard deviation more than 1% and the range about 5%. The worst case for the approximation of equation (3.14) also occurs for power 1.39 (Figure 4.7b) but with better performance compared to the approximation of equation (3.2) with standard deviation 0.63% and the range 2.89%. the approximation of equation (3.2) has a slightly better performance for lower power, $a = 0.63$ with standard deviation 0.04% and the range about 0.25% compared to 0.14% of standard deviation and 0.59% of range in the approximation of equation (3.14).



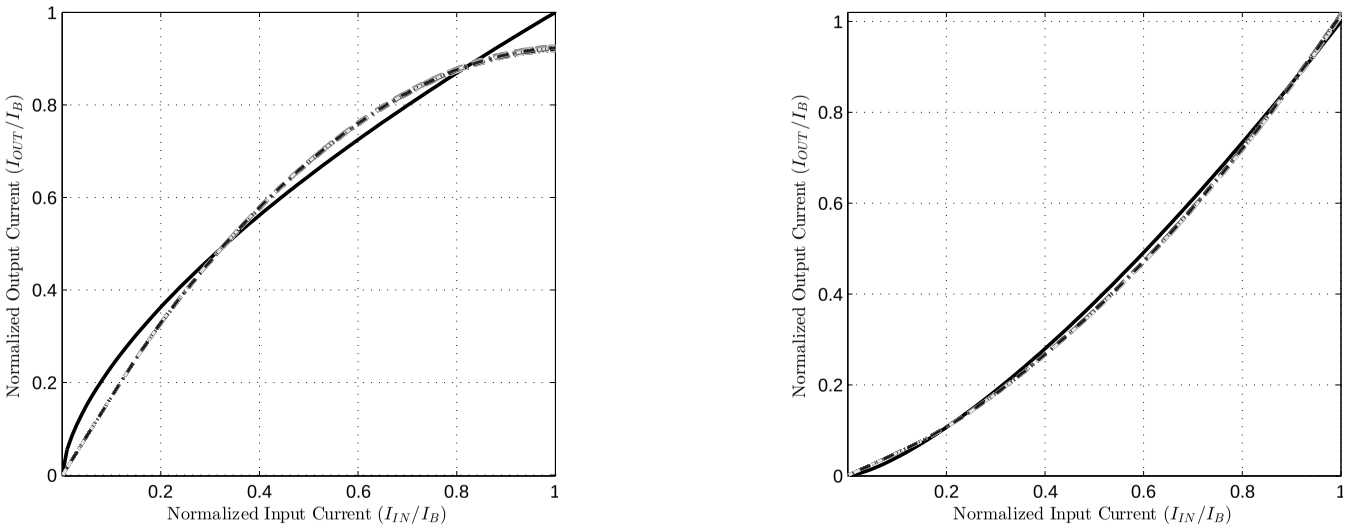
(a) $x^{0.19}$

(b) $x^{1.39}$

(c) $x^{1.91}$

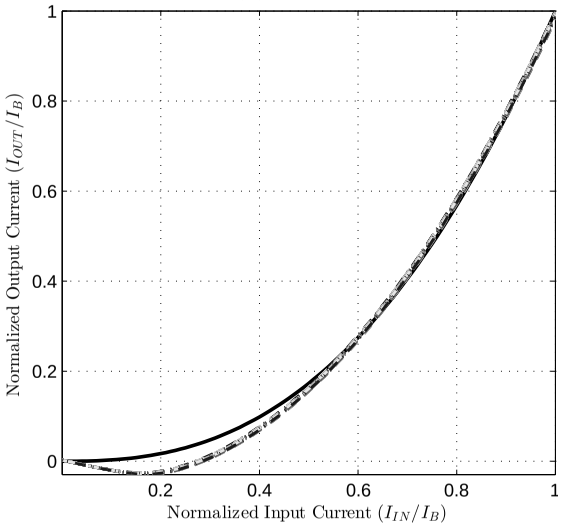
(d) $x^{3.00}$

Figure 4.5: Monte Carlo analysis of normalized output current with 3% transistor size variation of second order polynomial.

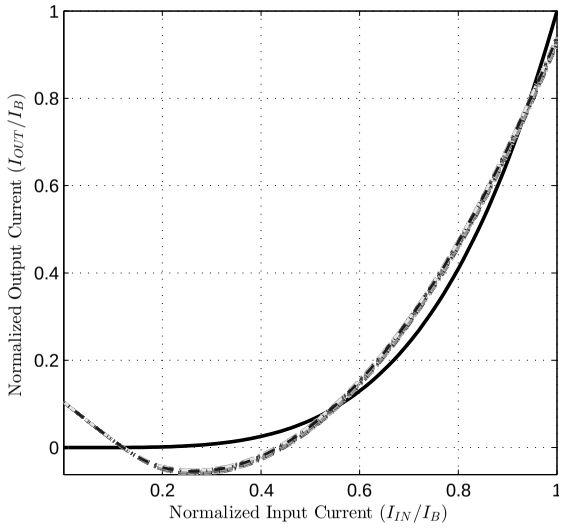


(a) $x^{0.63}$

(b) $x^{1.39}$



(c) $x^{2.53}$



(d) $x^{4.00}$

Figure 4.6: Monte Carlo analysis of normalized output current with 3% transistor size variation of second order polynomial without constant.

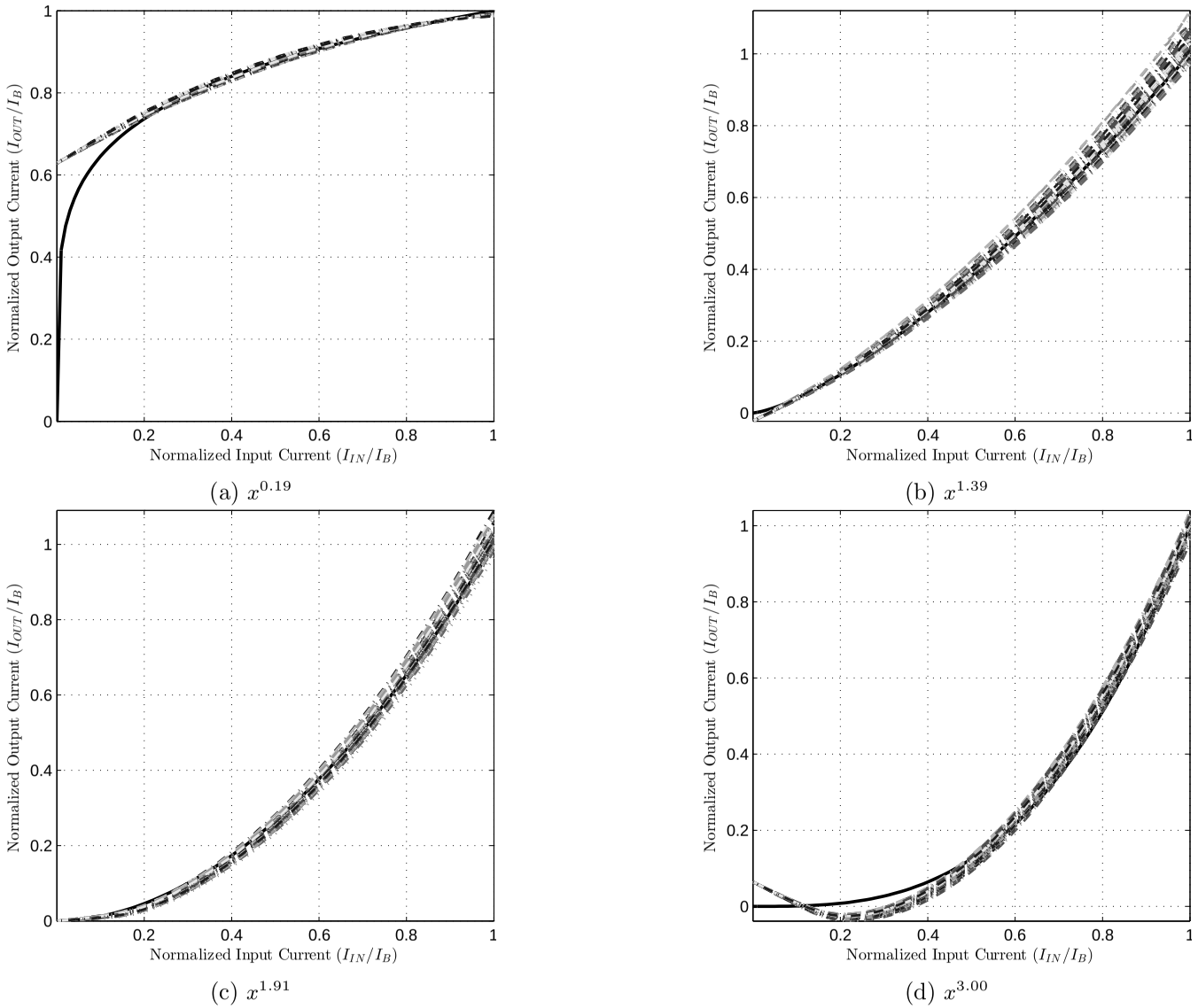
But in general, for this test, the approximation of equation (3.14) performs better than the approximation of equation (3.2).

Table 4.11: Monte Carlo analysis with 3% *tox* variation of second order polynomial approximation.

Power	RMSE						
	Typical	Max	Min	Mean	Median	Range	StdDev
0.19	7.26%	7.35%	7.24%	7.27%	7.26%	0.11%	0.02%
0.63	2.40%	2.62%	2.38%	2.42%	2.40%	0.25%	0.04%
0.90	0.37%	0.82%	0.36%	0.43%	0.40%	0.46%	0.08%
1.39	0.60%	5.66%	0.54%	1.44%	1.05%	5.12%	1.01%
1.91	1.06%	3.74%	0.97%	1.55%	1.37%	2.77%	0.57%
2.53	3.12%	5.06%	3.03%	3.23%	3.14%	2.03%	0.25%
3.00	2.85%	4.04%	2.69%	3.02%	2.92%	1.34%	0.30%
4.00	4.57%	5.41%	4.40%	4.59%	4.56%	1.01%	0.14%

Table 4.12: Monte Carlo analysis with 3% *tox* variation of second order polynomial approximation without constant.

Power	RMSE						
	Typical	Max	Min	Mean	Median	Range	StdDev
0.63	3.65%	4.22%	3.63%	3.75%	3.70%	0.59%	0.14%
0.90	0.64%	0.86%	0.58%	0.66%	0.65%	0.27%	0.06%
1.39	1.29%	3.89%	1.00%	1.71%	1.56%	2.89%	0.63%
1.91	1.28%	3.41%	1.22%	1.66%	1.49%	2.19%	0.43%
2.15	1.53%	2.19%	1.23%	1.58%	1.52%	0.96%	0.22%
2.53	2.17%	3.16%	2.09%	2.30%	2.26%	1.07%	0.17%
3.00	3.26%	3.53%	3.13%	3.28%	3.27%	0.40%	0.08%
4.00	5.38%	5.74%	5.28%	5.40%	5.39%	0.46%	0.09%



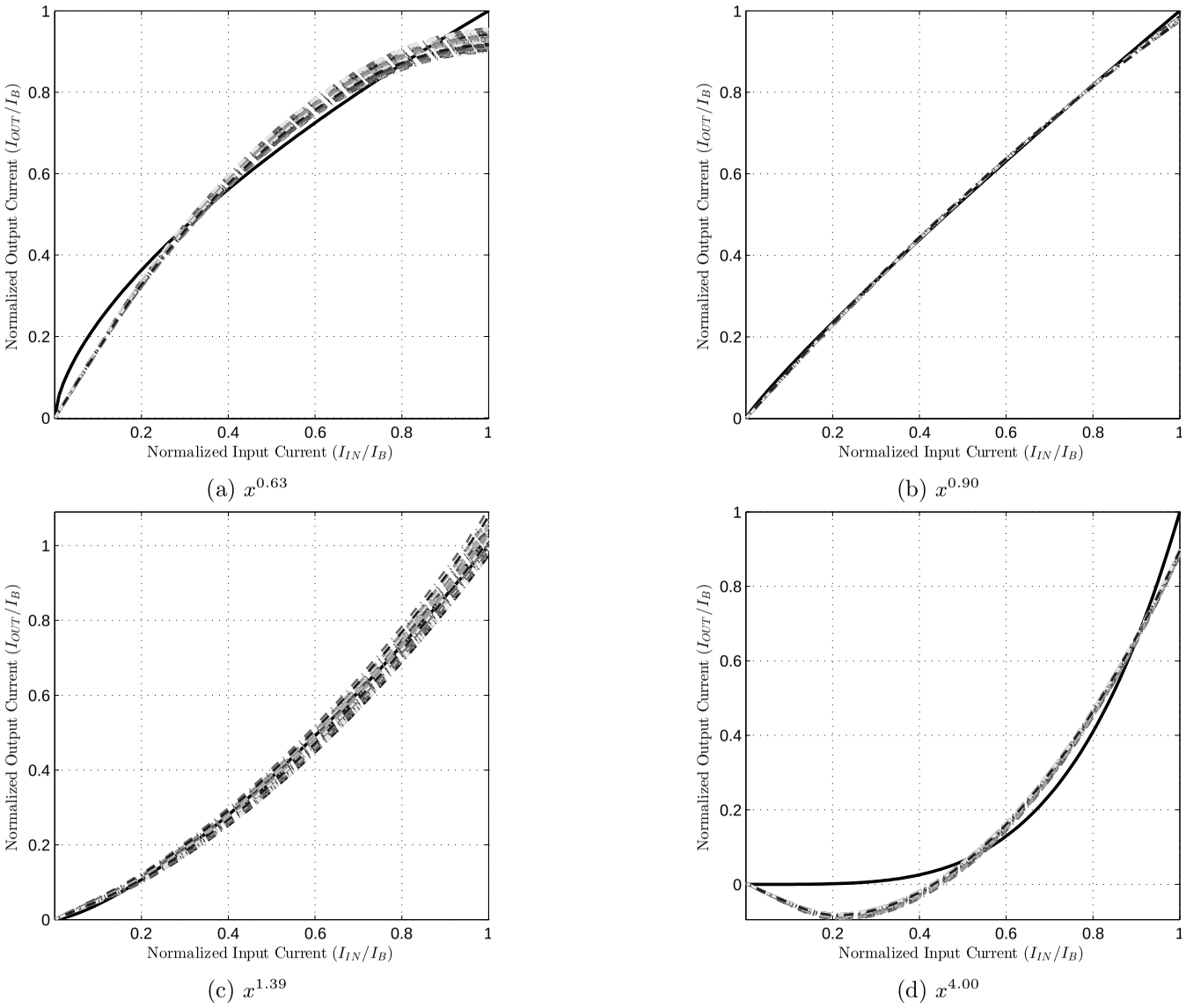
(a) $x^{0.19}$

(b) $x^{1.39}$

(c) $x^{1.91}$

(d) $x^{3.00}$

Figure 4.7: Monte Carlo analysis of normalized output current with 3% *tox* variation of second order polynomial approximation.



(a) $x^{0.63}$

(b) $x^{0.90}$

(c) $x^{1.39}$

(d) $x^{4.00}$

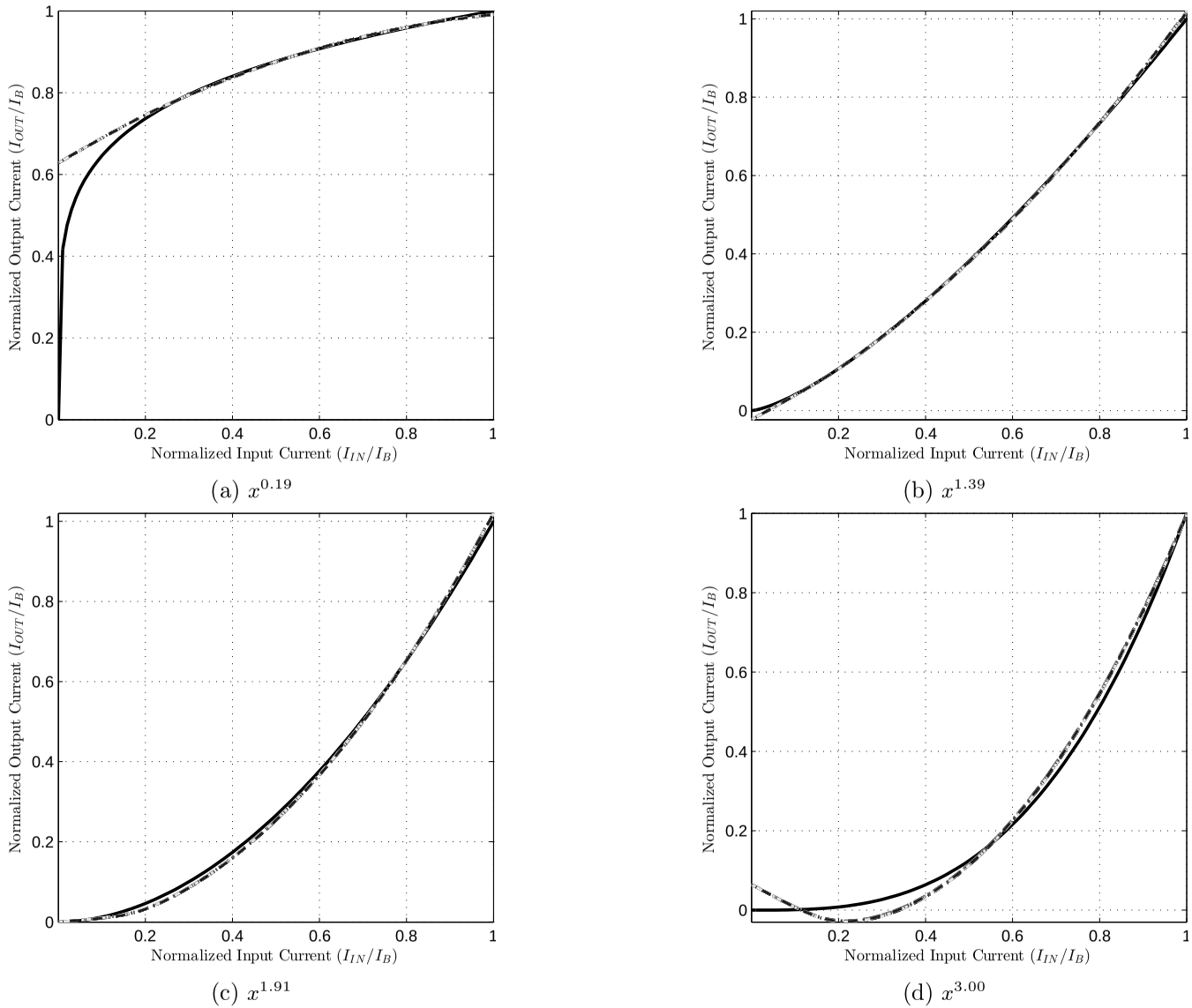
Figure 4.8: Monte Carlo analysis of normalized output current with 3% *tox* variation of second order polynomial approximation without constant.

Monte Carlo simulation by varying parameter $Vth0$

In this section, Monte Carlo simulation by varying parameter $Vth0$ of all the transistors by Gaussian distribution around 3% will be performed. The results are depicted in Figure 4.9 and 4.10. The statistical data of Monte Carlo simulation by varying parameter $Vth0$ of the transistors is presented on Tables 4.13 and 4.14. Inspection of the tables shows that the parameter voltage threshold ($Vth0$) provides the smallest sensitivity compared to the other two parameters before. The maximum standard deviation of RMSE is only 0.04 %. with the range of the maximum to minimum RMSE is not more than 0.18%. The standard deviation can be very near to zero for powers 0.19, 0.63, 0.90, 4.00 of the approximation of equation (3.2) and power 0.90 for the approximation of equation (3.14). By comparing standard deviation results for both approximation on Tables 4.13 and 4.14, it can be concluded that the approximation of equation (3.2) has better performance than the approximation of equation (3.14).

Table 4.13: Monte Carlo analysis with 3% $Vth0$ variation of the transistors second order polynomial approximation.

Power	RMSE						
	Typical	Max	Min	Mean	Median	Range	StdDev
0.19	7.26%	7.26%	7.25%	7.26%	7.26%	0.01%	0.00%
0.63	2.40%	2.41%	2.39%	2.40%	2.40%	0.01%	0.00%
0.90	0.37%	0.37%	0.36%	0.37%	0.37%	0.00%	0.00%
1.39	0.60%	0.63%	0.59%	0.60%	0.60%	0.04%	0.01%
1.91	1.06%	1.14%	0.98%	1.06%	1.06%	0.15%	0.03%
2.53	3.12%	3.13%	3.04%	3.08%	3.07%	0.09%	0.02%
3.00	2.85%	2.88%	2.83%	2.85%	2.85%	0.05%	0.01%
4.00	4.57%	4.59%	4.57%	4.57%	4.57%	0.03%	0.00%



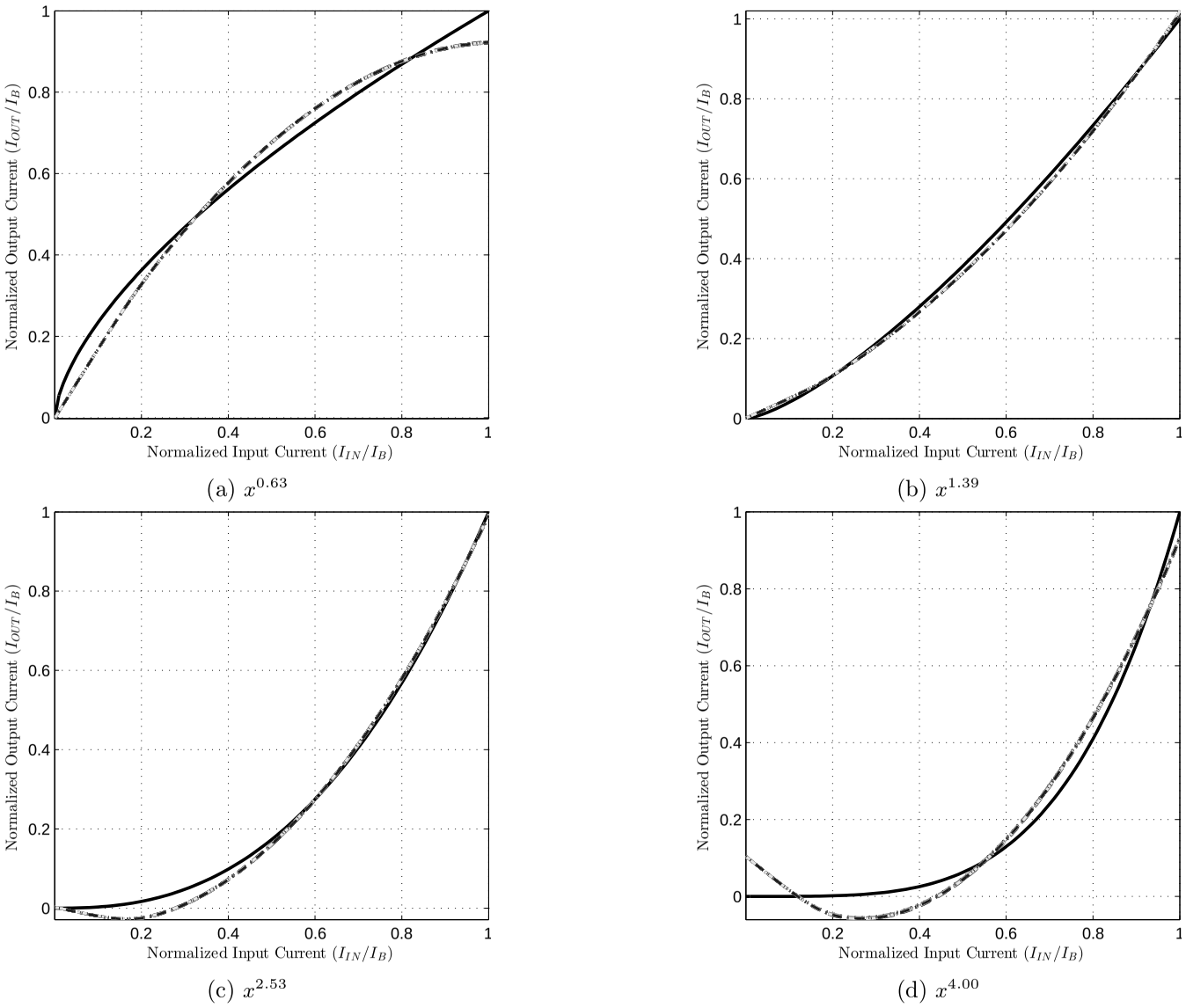
(a) $x^{0.19}$

(b) $x^{1.39}$

(c) $x^{1.91}$

(d) $x^{3.00}$

Figure 4.9: Monte Carlo analysis of normalized output current with 3% $Vth0$ variation of second order polynomial approximation.



(a) $x^{0.63}$

(b) $x^{1.39}$

(c) $x^{2.53}$

(d) $x^{4.00}$

Figure 4.10: Monte Carlo analysis of normalized output current with 3% $Vth0$ variation of second order polynomial approximation without constant.

Table 4.14: Monte Carlo analysis with 3% $Vth0$ variation of the transistors second order polynomial approximation without constant.

Power	RMSE						
	Typical	Max	Min	Mean	Median	Range	StdDev
0.63	3.65%	3.66%	3.63%	3.65%	3.65%	0.03%	0.01%
0.90	0.64%	0.67%	0.64%	0.65%	0.65%	0.03%	0.00%
1.39	1.29%	1.38%	1.22%	1.29%	1.28%	0.15%	0.03%
1.91	1.28%	1.36%	1.23%	1.28%	1.27%	0.13%	0.03%
2.15	1.53%	1.60%	1.46%	1.53%	1.53%	0.15%	0.03%
2.53	2.17%	2.26%	2.08%	2.17%	2.17%	0.18%	0.04%
3.00	3.26%	3.35%	3.20%	3.26%	3.25%	0.15%	0.03%
4.00	5.38%	5.42%	5.32%	5.37%	5.38%	0.10%	0.02%

Monte Carlo simulation by using built-in statistical parameter TSMC RF 180nm

In this section, Monte Carlo simulation by using the built-in statistical parameter defined by library of TSMC RF 180nm. will be performed This library has provided a set of variations of the process parameters defined by the foundry of TSMC to be used in Monte Carlo (MC) analysis. The results are depicted in Figures 4.11 and 4.12. The statistical data of Monte Carlo simulation by using built-in statistical library is presented on Tables 4.15 and 4.16.

The results show that the proposed circuit has some sensitivity to the process parameter variation for certain range especially between power more than 0.90 and lower than 3.00 for both approximations with standard deviation of RMSE more than 0.1% and the range is more than 0.5%. The highest sensitivity for both approximations occurs at power 1.39. the approximation of equation (3.2) (Figure 4.11b) has 0.27% of standard deviation and 1.26% of range, and the approximation of equation (3.14) (Figure 4.12b) has 0.31% of standard deviation and 1.16% of range. However for lower

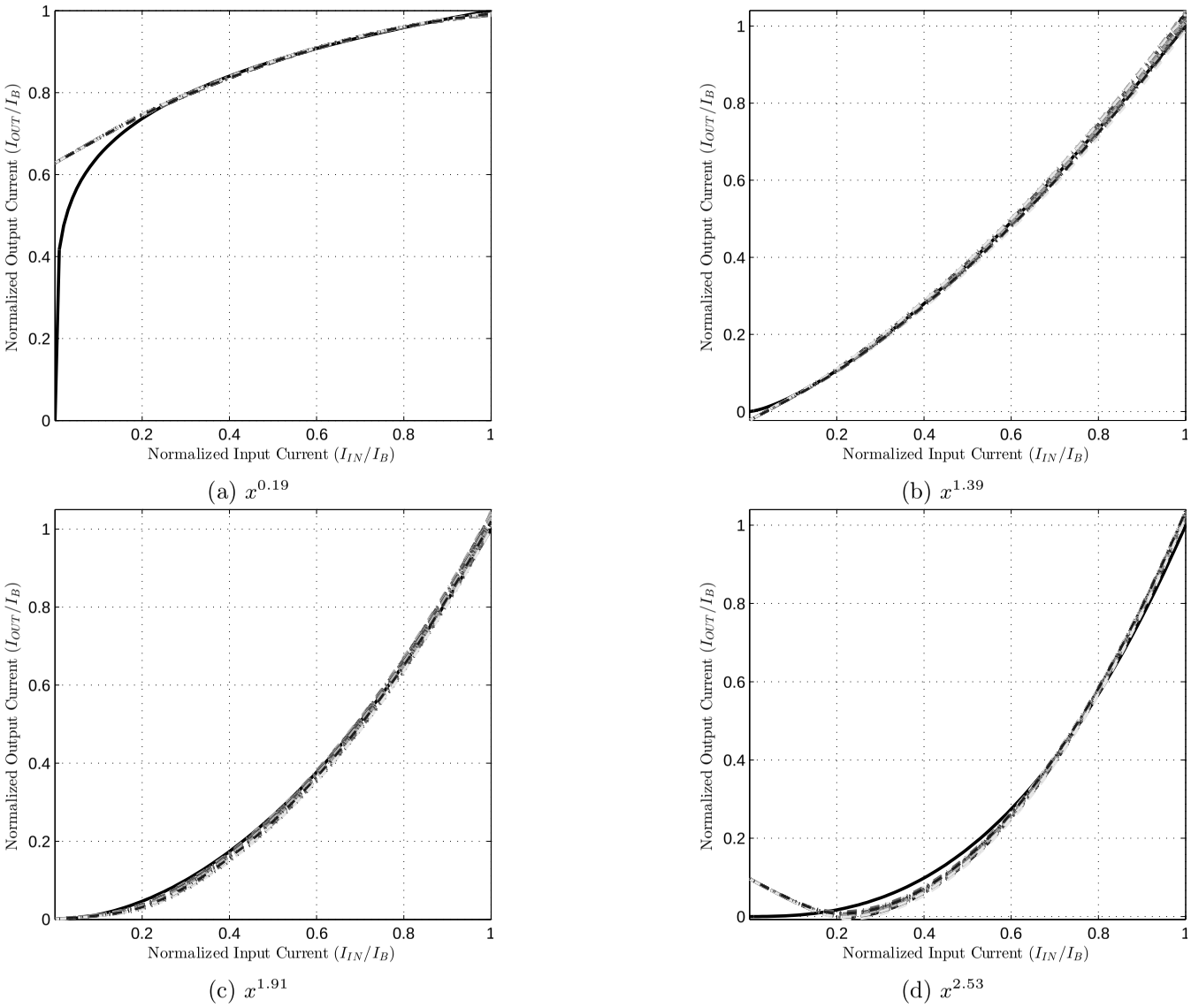
power (0.19, 0.63, and 0.90) the standard deviation is very low; for the approximation of equation (3.2) it is only 0.01% and 0.02% for the approximation of equation (3.14). The approximation of equation (3.14) only has better performance for power 1.91 with 0.17% of standard deviation and 0.98% of range compared to 0.22% of standard deviation and 1.15% of range for the approximation of equation (3.2). But generally, the approximation of equation (3.2) has better performance compared to the approximation of equation (3.14).

Table 4.15: Monte Carlo analysis by using built-in statistical library of second order polynomial approximation.

Power	RMSE						
	Typical	Max	Min	Mean	Median	Range	StdDev
0.19	7.26%	7.28%	7.24%	7.25%	7.26%	0.04%	0.01%
0.63	2.40%	2.43%	2.38%	2.40%	2.40%	0.05%	0.01%
0.90	0.37%	0.45%	0.36%	0.37%	0.37%	0.10%	0.01%
1.39	0.60%	1.78%	0.52%	0.80%	0.72%	1.26%	0.27%
1.91	1.06%	2.01%	0.86%	1.18%	1.14%	1.15%	0.22%
2.53	3.12%	3.53%	2.91%	3.09%	3.07%	0.62%	0.10%
3.00	2.85%	3.04%	2.71%	2.87%	2.87%	0.32%	0.06%
4.00	4.57%	4.81%	4.44%	4.60%	4.60%	0.37%	0.07%

Table 4.16: Monte Carlo analysis by using built-in statistical library of second order polynomial approximation without constant.

Power	RMSE						
	Typical	Max	Min	Mean	Median	Range	StdDev
0.63	3.65%	3.71%	3.62%	3.66%	3.65%	0.08%	0.02%
0.90	0.64%	0.70%	0.62%	0.66%	0.65%	0.08%	0.02%
1.39	1.29%	2.14%	0.98%	1.36%	1.27%	1.16%	0.31%
1.91	1.28%	2.09%	1.12%	1.37%	1.34%	0.98%	0.17%
2.15	1.53%	1.88%	1.29%	1.54%	1.53%	0.59%	0.13%
2.53	2.17%	2.55%	1.91%	2.20%	2.17%	0.64%	0.13%
3.00	3.26%	3.59%	2.97%	3.25%	3.22%	0.62%	0.10%
4.00	5.38%	5.58%	5.18%	5.37%	5.36%	0.40%	0.09%



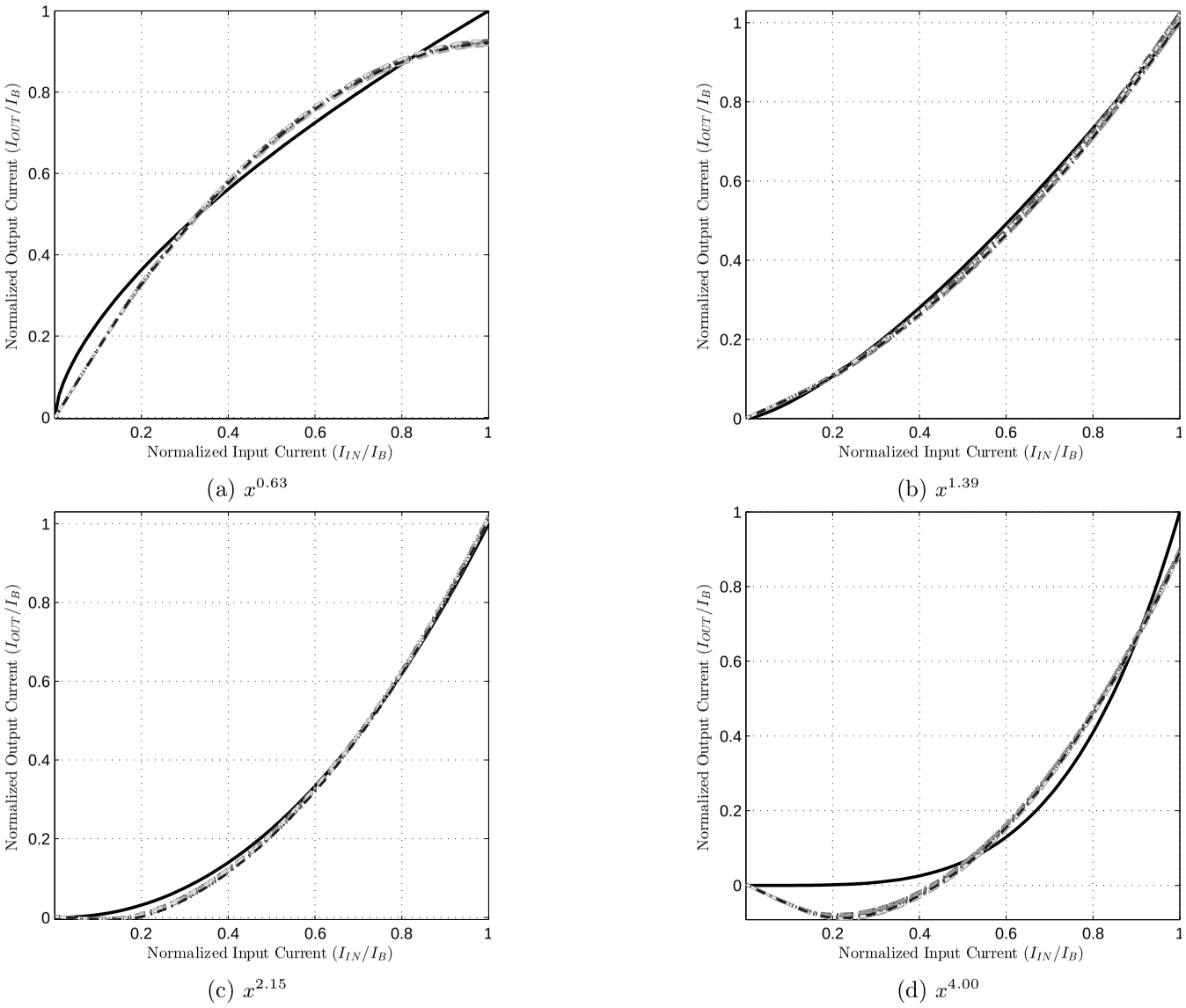
(a) $x^{0.19}$

(b) $x^{1.39}$

(c) $x^{1.91}$

(d) $x^{2.53}$

Figure 4.11: Monte Carlo analysis of normalized output current by using built-in statistical parameter of second order polynomial approximation.



(a) $x^{0.63}$

(b) $x^{1.39}$

(c) $x^{2.15}$

(d) $x^{4.00}$

Figure 4.12: Monte Carlo analysis of normalized output current by using built-in statistical parameter of second order polynomial approximation without constant.

4.4 The Layout of the proposed circuits

In order to examine the feasibility of the fabrication of the proposed circuits, L-EDIT v16.3 is used to design the layout. The layout of the proposed circuit (without pads) is depicted in Figure 4.14. It used typical PMOS and NMOS transistors with two layers of metal 1 and metal 2 as the connection. The dimensions of the layout is approximately $25.553\mu m$ in height and $138.005\mu m$ in width. Layout Versus Schematics (LVS) test confirms that the layout design has equivalent topology (including geometry, size, and connection) with the schematic of Figure 4.13. Unfortunately, the definition file to extract the parasitic resistance and capacitance is not available. Figures 4.15 and 4.16 show some example results of the extracted layout to the Spice netlist (without parasitic resistance and capacitance) which is comparable with Figures 4.1.

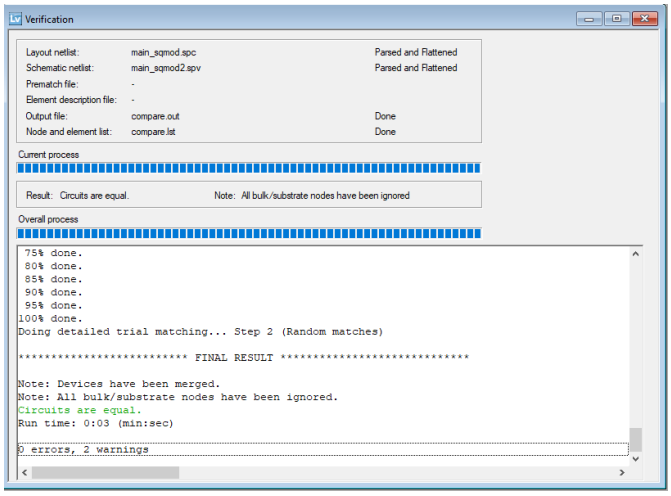


Figure 4.13: LVS test verify topology of the layout match with the schematics.

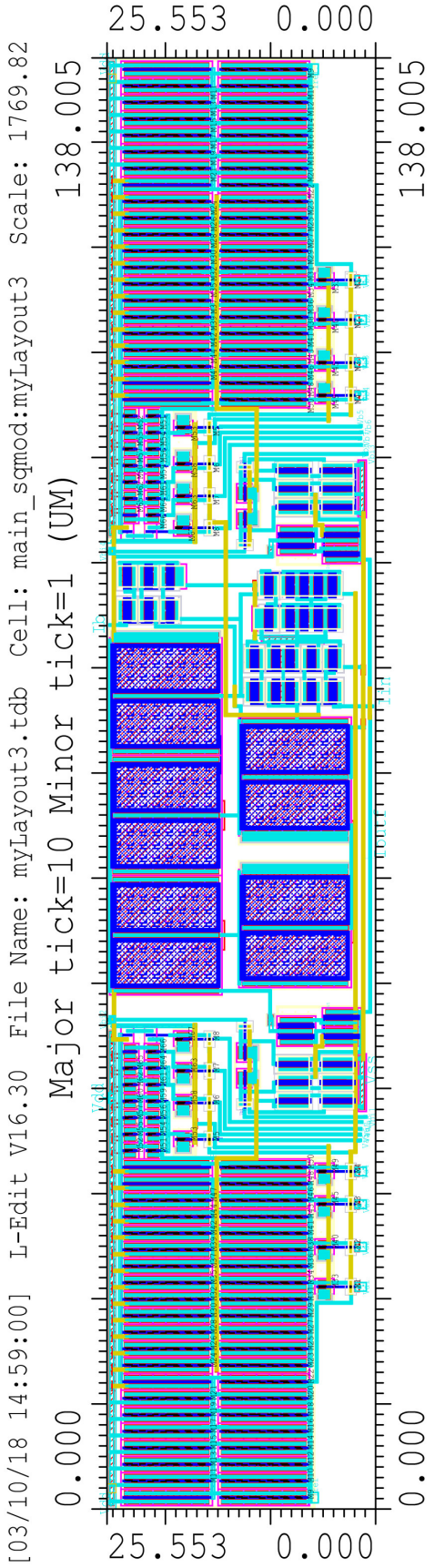
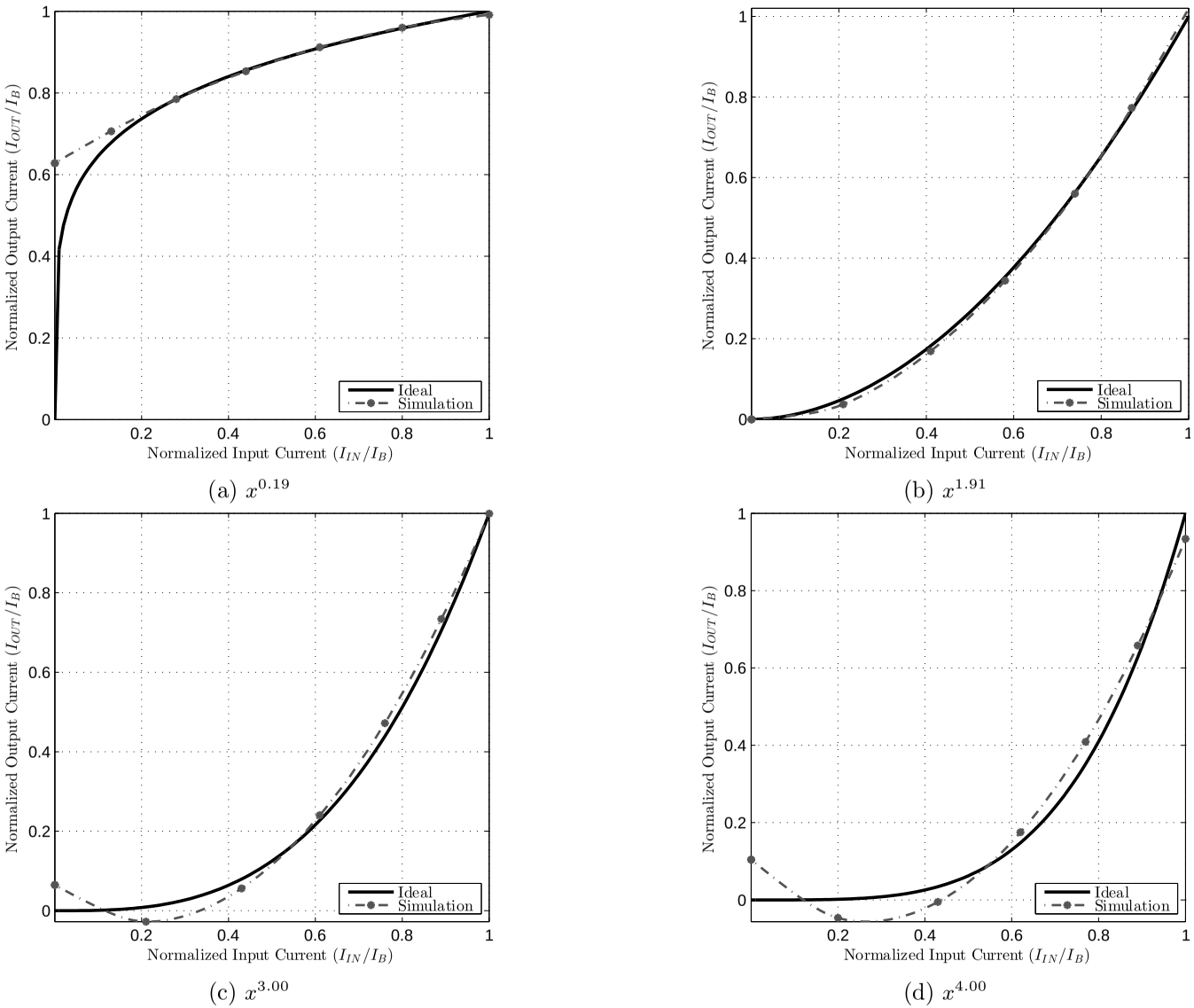


Figure 4.14: Layout design of the proposed circuit.



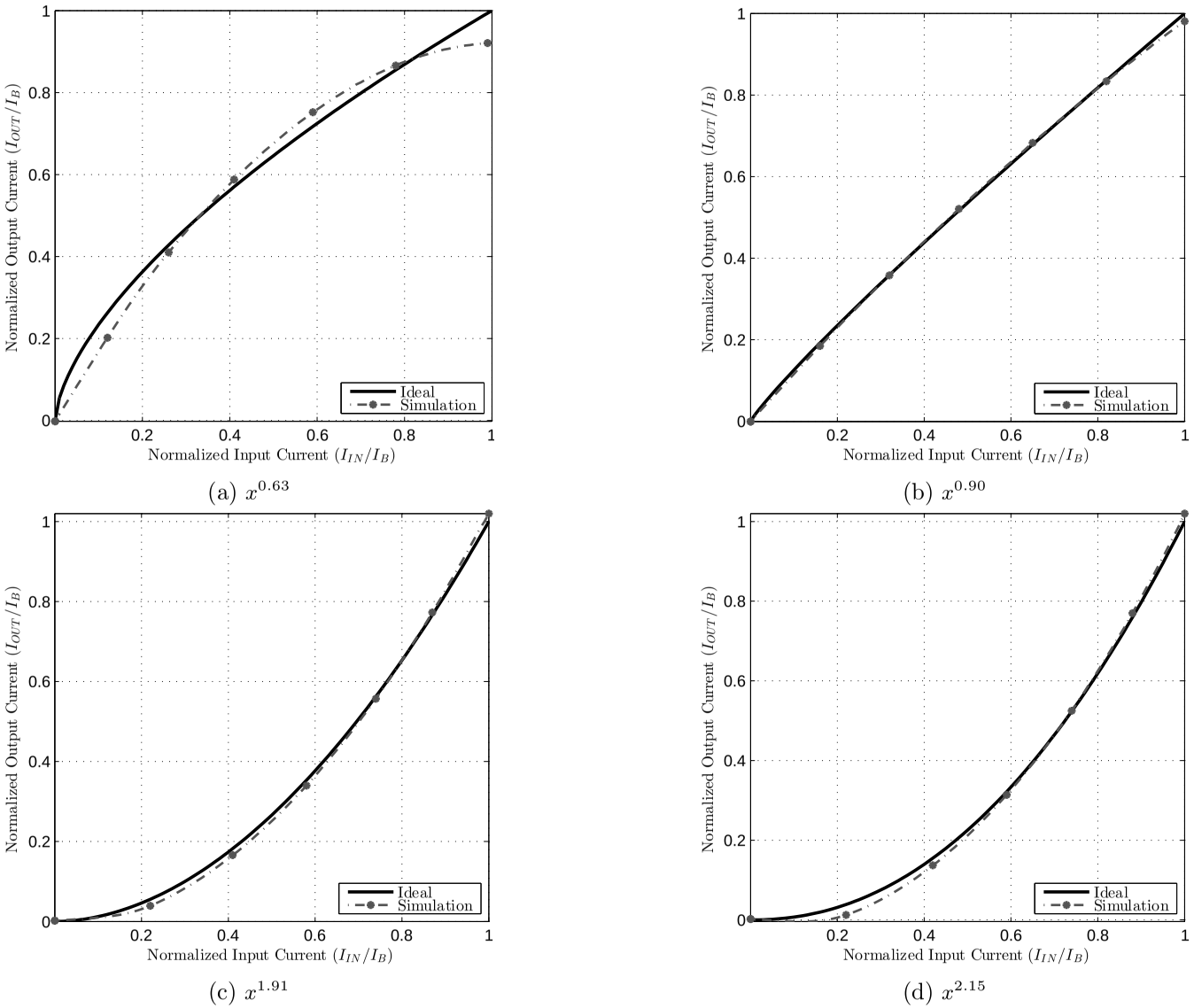
(a) $x^{0.19}$

(b) $x^{1.91}$

(c) $x^{3.00}$

(d) $x^{4.00}$

Figure 4.15: Post-layout simulation result of second order polynomial approximation



(a) $x^{0.63}$

(b) $x^{0.90}$

(c) $x^{1.91}$

(d) $x^{2.15}$

Figure 4.16: Post-layout simulation result of second order polynomial approximation without constant

4.5 The performance comparison with the previous works

The comparison of this work with the previous work of rational power functions generator are compiled in Table 4.17. This work has the largest error compared to the others about 7%. The error occurs in the big offset of low power ($a = 0.19$) in the range of input of $0 - 2\mu A$. In compensation with the error, it has lower power consumption with respect to the others works where transistors are working in saturation region. In this work the area occupied on the chip is smaller, and the range of the power is wider, as it covers the range 0-4. This work uses newer technology $0.18\mu m$ and dual voltage supply, VDD=-VSS=1.25V rather than use only single voltage supply like the others, which provides compatibility in integration to another Integrated Circuit (IC).

Table 4.17: The compilation of simulation results of some proposed rational powered function generator with this work.

Comparison Factors	[4]	[6]	[7]	[8]	[9, 10]	[12]	[5]	This work
Year	1998	2002	2007	2010	2011	2012	2017	2018
Technology (um)	n/a	0.35	0.35	0.35	0.35	0.35	0.18	0.18
Power Supply (V)	+-5	3.3	3.3	3.3	3.3	2.5	0.5	±1.25
Maximum Power consumption (uW)	n/a	n/a	5000	1050	800	970	0.48	410
Programming Codes (bits)	n/a	8	15	7	8	3	n/a	8
Power Resolution	n/m	Some limited power	0.125	0.03125	Continuous (0-2)	n/m	$\pm n/m$	Continous (0-4)
RMS Error (%)	< 3	n/a	1.32	1.45	1.25	3	1.05	7.3
Size Layout (mm^2)	n/a	Core:1.55 Total:6.81	n/a	n/a	0.045	n/a	n/a	0.0035
Approximation	No	No	No	Yes	Yes	Yes	No	Yes
Research Type	Simulation	Fabrication	Simulation	Simulation	Simulation	Fabrication	Simulation	Simulation
Method	BJT, OpAmp, TLP	Cascade G-mean and Sq/d	Improved Cascade	MTL	MTL	MTL	FGMOS, Sub-threshold	MTL

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

In this thesis, a new approach to approximate rational-powered functions generator has been presented. The current-mode implementation of the proposed approximations using CMOS transistors working in the saturation region has also been presented. The new approximations use only squaring function and avoid the use of square-rooting function. Thus, it is consuming less power and less area on the chip.

The proposed circuit offers two kind of approximation. The first approximation uses a linear term, a squaring term, and a DC component. It generally has better performance in terms of RMSE, sustainability to temperature and parameters variations, and wider range of the rational-powered functions that can be implemented compared to the second approximation. However, there are zero offset and negative offset problems to be taking care of.

The second approximation uses only two terms: a linear term and a squaring term. offers lower power consumption and significantly reduces zero offset and negative offset in the range of powers 0.63-2.15. This two approach exploit the same circuit, hence the

user has a flexibility to select which approximation and the range of the power will be used by controlling the gain of each terms.

The layout design of the proposed circuit has been carried out to check the feasibility to fabricate the circuit. The size of the layout is $25.553\mu m \times 138.005\mu m$. Compared to previous works, this work has larger maximum RMSE about 7%. However, it uses compatible dual voltage supply, newer technology, consumes less power, and less area on chip.

5.2 Recommendation

There is always a door for improvement. The author recommends some points that can be considered as an extension to this work:

- Fabricating the designed circuits and testing them
- Developing technique to improve the performance of the squaring circuit under process variation and temperature variation.
- Looking for another technique for circuit design approaches other than MTL approach.

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Vitae

- Name: Adi Kurniawan
- Nationality: Indonesian
- Date of Birth: May 28th, 1989
- Email: *kurniawan2805@gmail.com*
- Permenant Address: Jalan Caladi 57, Sadang Serang, Coblong, Bandung 40133
- Academic Background:
  - Masters of Science in Electrical Engineering, King Fahd University of Petroleum and Minerals (KFUPM), Saudi Arabia, April 2018
  - Bachelors of Engineering in Electrical Engineering, Institut Teknologi Bandung (ITB), Bandung, Indonesia, June 2012
- Research Experience:
  - 50k Competition: Smart Water Ablution Recycle (2015-2016)
  - Undergraduate Final Project: Development of RSA FPGA-based for VoIP application resistant to Side Channel Attack (2011-2012)
  - Implementation of Very Simple Radix-2 Single Path Delay Configurable Fast Fourier Transform (FFT) (2011-2012)